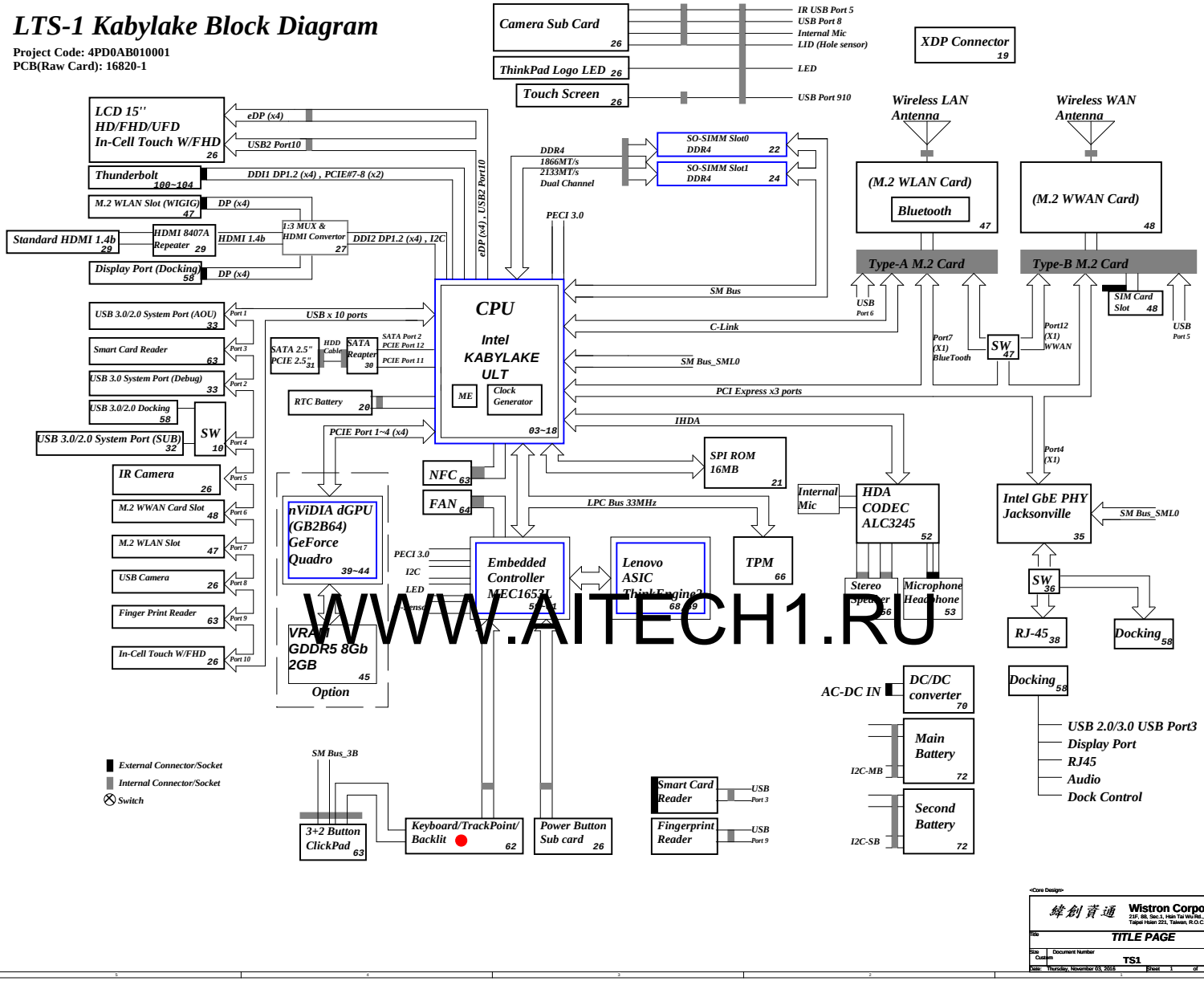
LTS-1 Kabylake Block Diagram

Project Code: 4PD0AB010001
PCB(Raw Card): 16820-1



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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title: TITLE PAGE
Size: Custom | Document Number: TS1 | Rev: 1
Date: Thursday, November 03, 2016 | Sheet 1 of 103

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Title: EC HISTORY

Size	Document Number	Rev
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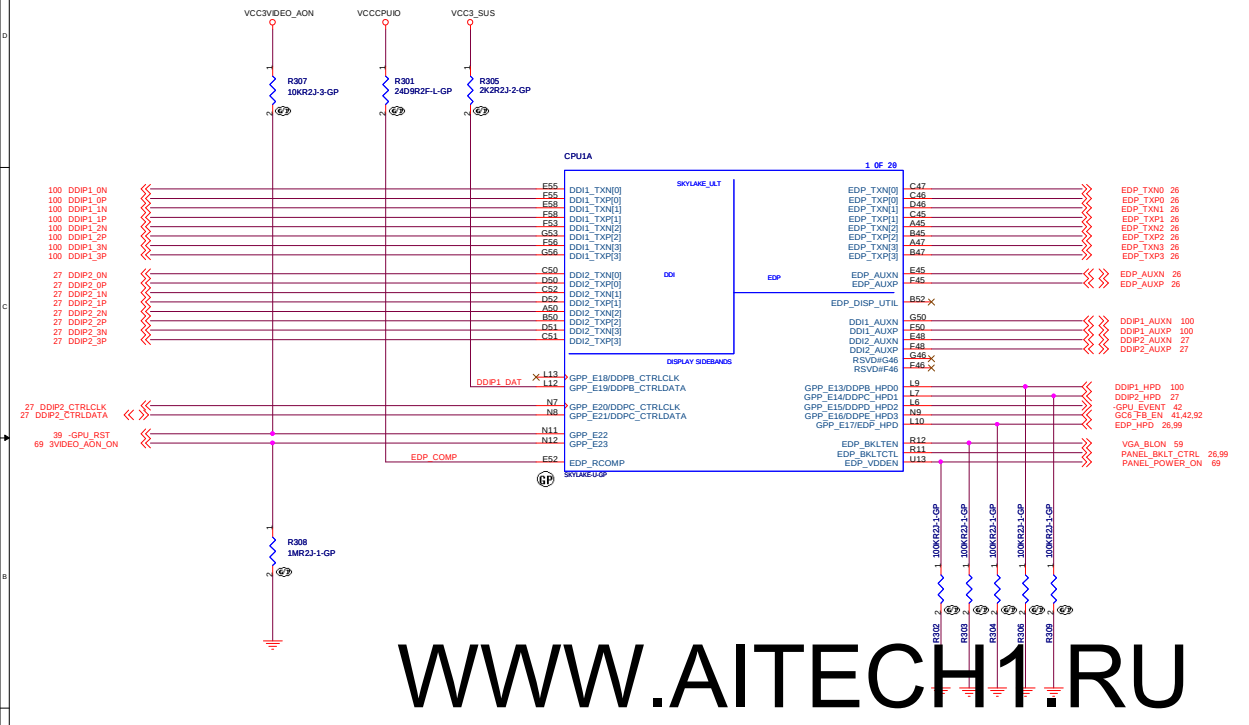
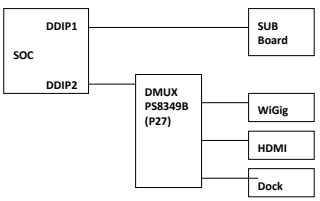


TABLE: Functional Strap

DDPB_CTRLDATA	
HIGH	Port B is detected.
LOW	Port B is not detected.
DDPC_CTRLDATA	
HIGH	Port C is detected.
LOW	Port C is not detected.



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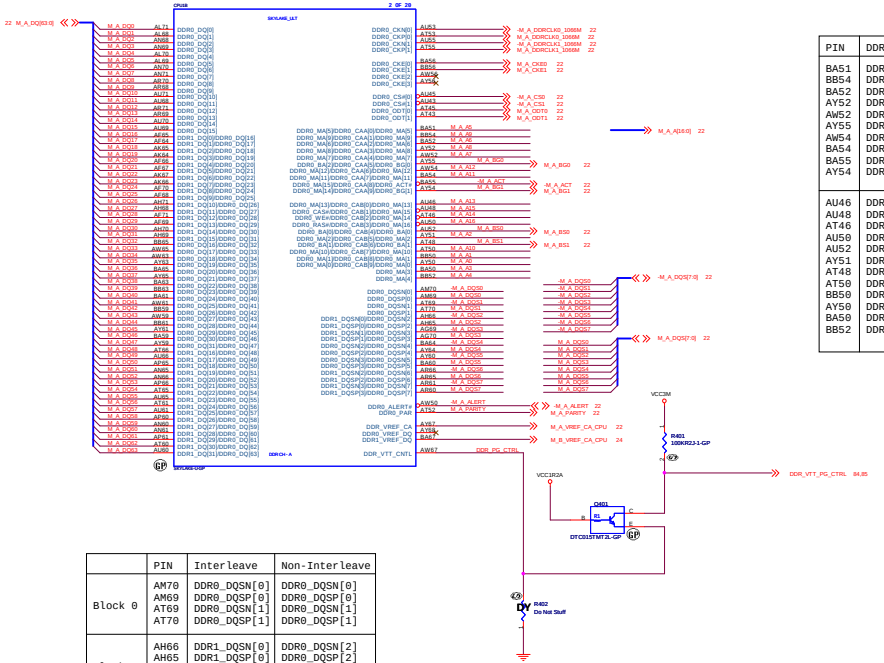
Title: CPU(1/16) : DDI/EDP

Size	Document Number	Rev
A3	TS1	1

Date: Thursday, November 03, 2016 Sheet 3 of 103

	PIN	Interleave	Non-Interleave
Block 0	AL71	DDR0_DQ[0]	DDR0_DQ[0]
	AL68	DDR0_DQ[1]	DDR0_DQ[1]
	AN68	DDR0_DQ[2]	DDR0_DQ[2]
	AN69	DDR0_DQ[3]	DDR0_DQ[3]
	AL70	DDR0_DQ[4]	DDR0_DQ[4]
	AL69	DDR0_DQ[5]	DDR0_DQ[5]
	AN70	DDR0_DQ[6]	DDR0_DQ[6]
	AN71	DDR0_DQ[7]	DDR0_DQ[7]
	AR70	DDR0_DQ[8]	DDR0_DQ[8]
	AR68	DDR0_DQ[9]	DDR0_DQ[9]
	AU71	DDR0_DQ[10]	DDR0_DQ[10]
	AU68	DDR0_DQ[11]	DDR0_DQ[11]
	AR71	DDR0_DQ[12]	DDR0_DQ[12]
	AR69	DDR0_DQ[13]	DDR0_DQ[13]
	AU70	DDR0_DQ[14]	DDR0_DQ[14]
	AU69	DDR0_DQ[15]	DDR0_DQ[15]
Block 1	AF65	DDR1_DQ[0]	DDR0_DQ[16]
	AF64	DDR1_DQ[1]	DDR0_DQ[17]
	AK65	DDR1_DQ[2]	DDR0_DQ[18]
	AK64	DDR1_DQ[3]	DDR0_DQ[19]
	AF66	DDR1_DQ[4]	DDR0_DQ[20]
	AF67	DDR1_DQ[5]	DDR0_DQ[21]
	AK67	DDR1_DQ[6]	DDR0_DQ[22]
	AK66	DDR1_DQ[7]	DDR0_DQ[23]
	AF70	DDR1_DQ[8]	DDR0_DQ[24]
	AF68	DDR1_DQ[9]	DDR0_DQ[25]
	AH71	DDR1_DQ[10]	DDR0_DQ[26]
	AH68	DDR1_DQ[11]	DDR0_DQ[27]
	AF71	DDR1_DQ[12]	DDR0_DQ[28]
	AF69	DDR1_DQ[13]	DDR0_DQ[29]
	AH70	DDR1_DQ[14]	DDR0_DQ[30]
	AH69	DDR1_DQ[15]	DDR0_DQ[31]
Block 2	BB65	DDR0_DQ[16]	DDR0_DQ[32]
	AW65	DDR0_DQ[17]	DDR0_DQ[33]
	AW63	DDR0_DQ[18]	DDR0_DQ[34]
	AY63	DDR0_DQ[19]	DDR0_DQ[35]
	BA65	DDR0_DQ[20]	DDR0_DQ[36]
	AY65	DDR0_DQ[21]	DDR0_DQ[37]
	BA63	DDR0_DQ[22]	DDR0_DQ[38]
	BB63	DDR0_DQ[23]	DDR0_DQ[39]
	BA61	DDR0_DQ[24]	DDR0_DQ[40]
	AW61	DDR0_DQ[25]	DDR0_DQ[41]
	BB59	DDR0_DQ[26]	DDR0_DQ[42]
	AW59	DDR0_DQ[27]	DDR0_DQ[43]
	BB61	DDR0_DQ[28]	DDR0_DQ[44]
	AY61	DDR0_DQ[29]	DDR0_DQ[45]
	BA59	DDR0_DQ[30]	DDR0_DQ[46]
	AY59	DDR0_DQ[31]	DDR0_DQ[47]
Block 3	AT66	DDR1_DQ[16]	DDR0_DQ[48]
	AU66	DDR1_DQ[17]	DDR0_DQ[49]
	AP65	DDR1_DQ[18]	DDR0_DQ[50]
	AN65	DDR1_DQ[19]	DDR0_DQ[51]
	AN66	DDR1_DQ[20]	DDR0_DQ[52]
	AP66	DDR1_DQ[21]	DDR0_DQ[53]
	AT65	DDR1_DQ[22]	DDR0_DQ[54]
	AU65	DDR1_DQ[23]	DDR0_DQ[55]
	AT61	DDR1_DQ[24]	DDR0_DQ[56]
	AU61	DDR1_DQ[25]	DDR0_DQ[57]
	AP60	DDR1_DQ[26]	DDR0_DQ[58]
	AN60	DDR1_DQ[27]	DDR0_DQ[59]
	AN61	DDR1_DQ[28]	DDR0_DQ[60]
	AP61	DDR1_DQ[29]	DDR0_DQ[61]
	AT60	DDR1_DQ[30]	DDR0_DQ[62]
	AU60	DDR1_DQ[31]	DDR0_DQ[63]

LOGIC



	PIN	Interleave	Non-Interleave
Block 0	AM70	DDR0_DQSN[0]	DDR0_DQSN[0]
	AM69	DDR0_DQSP[0]	DDR0_DQSP[0]
	AT69	DDR0_DQSN[1]	DDR0_DQSN[1]
	AT70	DDR0_DQSP[1]	DDR0_DQSP[1]
Block 1	AH66	DDR1_DQSN[0]	DDR0_DQSN[2]
	AH65	DDR1_DQSP[0]	DDR0_DQSP[2]
	AG69	DDR1_DQSN[1]	DDR0_DQSN[3]
	AG68	DDR1_DQSP[1]	DDR0_DQSP[3]
Block 2	BA64	DDR0_DQSN[2]	DDR0_DQSN[4]
	BA64	DDR0_DQSP[2]	DDR0_DQSP[4]
	AY60	DDR0_DQSN[3]	DDR0_DQSN[5]
	BA60	DDR0_DQSP[3]	DDR0_DQSP[5]
Block 3	AR66	DDR1_DQSN[2]	DDR0_DQSN[6]
	AR65	DDR1_DQSP[2]	DDR0_DQSP[6]
	AR61	DDR1_DQSN[3]	DDR0_DQSN[7]
	AR60	DDR1_DQSP[3]	DDR0_DQSP[7]

LOGIC

PIN	DDR3L	LPDDR3	DDR4
BA51	DDR0_MA[5]	DDR0_CAA[0]	DDR0_MA[5]
BB54	DDR0_MA[9]	DDR0_CAA[1]	DDR0_MA[9]
BA52	DDR0_MA[6]	DDR0_CAA[2]	DDR0_MA[6]
AY52	DDR0_MA[8]	DDR0_CAA[3]	DDR0_MA[8]
AW52	DDR0_MA[7]	DDR0_CAA[4]	DDR0_MA[7]
AY55	DDR0_BA[2]	DDR0_CAA[5]	DDR0_BG[0]
AW54	DDR0_MA[12]	DDR0_CAA[6]	DDR0_MA[12]
BA54	DDR0_MA[11]	DDR0_CAA[7]	DDR0_MA[11]
BA55	DDR0_MA[15]	DDR0_CAA[8]	DDR0_ACT#
AY54	DDR0_MA[14]	DDR0_CAA[9]	DDR0_BG[1]
AU46	DDR0_MA[13]	DDR0_CAB[0]	DDR0_MA[13]
AU48	DDR0_CAS#	DDR0_CAB[1]	DDR0_MA[15]
AT46	DDR0_WE#	DDR0_CAB[2]	DDR0_MA[14]
AU50	DDR0_RAS#	DDR0_CAB[3]	DDR0_MA[16]
AU52	DDR0_BA[0]	DDR0_CAB[4]	DDR0_BA[0]
AY51	DDR0_MA[2]	DDR0_CAB[5]	DDR0_MA[2]
AT48	DDR0_BA[1]	DDR0_CAB[6]	DDR0_BA[1]
AT50	DDR0_MA[10]	DDR0_CAB[7]	DDR0_MA[10]
BB50	DDR0_MA[1]	DDR0_CAB[8]	DDR0_MA[1]
AY50	DDR0_MA[0]	DDR0_CAB[9]	DDR0_MA[0]
BA50	DDR0_MA[3]	Not Used	DDR0_MA[3]
BB52	DDR0_MA[4]	Not Used	DDR0_MA[4]

LOGIC

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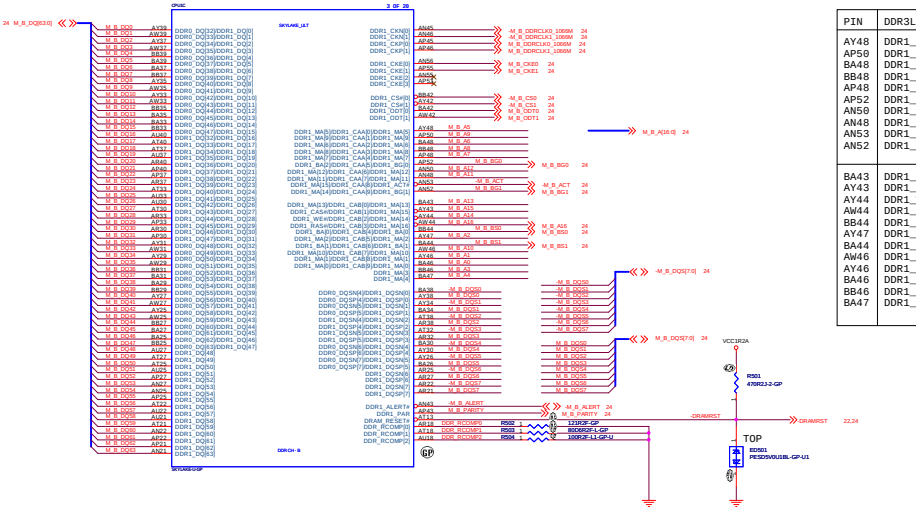
Title	CPU(2/16) : DDR CHANNEL-A
Size: A2	Document Number: TS1
Date: Thursday, November 03, 2016	Sheet 4 of 100

	PIN	Interleave	Non-Interleave
Block 4	AY39	DDR0_DQ[32]	DDR1_DQ[0]
	AW39	DDR0_DQ[33]	DDR1_DQ[1]
	AY37	DDR0_DQ[34]	DDR1_DQ[2]
	AW37	DDR0_DQ[35]	DDR1_DQ[3]
	BB39	DDR0_DQ[36]	DDR1_DQ[4]
	BA39	DDR0_DQ[37]	DDR1_DQ[5]
	BA37	DDR0_DQ[38]	DDR1_DQ[6]
	BB37	DDR0_DQ[39]	DDR1_DQ[7]
	AY35	DDR0_DQ[40]	DDR1_DQ[8]
	AW35	DDR0_DQ[41]	DDR1_DQ[9]
	AY33	DDR0_DQ[42]	DDR1_DQ[10]
	AW33	DDR0_DQ[43]	DDR1_DQ[11]
	BB35	DDR0_DQ[44]	DDR1_DQ[12]
	BA35	DDR0_DQ[45]	DDR1_DQ[13]
	BA33	DDR0_DQ[46]	DDR1_DQ[14]
	BB33	DDR0_DQ[47]	DDR1_DQ[15]
Block 5	AU40	DDR1_DQ[32]	DDR1_DQ[16]
	AT40	DDR1_DQ[33]	DDR1_DQ[17]
	AT37	DDR1_DQ[34]	DDR1_DQ[18]
	AU37	DDR1_DQ[35]	DDR1_DQ[19]
	AR40	DDR1_DQ[36]	DDR1_DQ[20]
	AP40	DDR1_DQ[37]	DDR1_DQ[21]
	AP37	DDR1_DQ[38]	DDR1_DQ[22]
	AR37	DDR1_DQ[39]	DDR1_DQ[23]
	AT33	DDR1_DQ[40]	DDR1_DQ[24]
	AU33	DDR1_DQ[41]	DDR1_DQ[25]
	AU30	DDR1_DQ[42]	DDR1_DQ[26]
	AT30	DDR1_DQ[43]	DDR1_DQ[27]
	AR33	DDR1_DQ[44]	DDR1_DQ[28]
	AP33	DDR1_DQ[45]	DDR1_DQ[29]
	AR30	DDR1_DQ[46]	DDR1_DQ[30]
	AP30	DDR1_DQ[47]	DDR1_DQ[31]
Block 6	AY31	DDR0_DQ[48]	DDR1_DQ[32]
	AW31	DDR0_DQ[49]	DDR1_DQ[33]
	AY29	DDR0_DQ[50]	DDR1_DQ[34]
	AW29	DDR0_DQ[51]	DDR1_DQ[35]
	BB31	DDR0_DQ[52]	DDR1_DQ[36]
	BA31	DDR0_DQ[53]	DDR1_DQ[37]
	BA29	DDR0_DQ[54]	DDR1_DQ[38]
	BB29	DDR0_DQ[55]	DDR1_DQ[39]
	AY27	DDR0_DQ[56]	DDR1_DQ[40]
	AW27	DDR0_DQ[57]	DDR1_DQ[41]
	AY25	DDR0_DQ[58]	DDR1_DQ[42]
	AW25	DDR0_DQ[59]	DDR1_DQ[43]
	BB27	DDR0_DQ[60]	DDR1_DQ[44]
	BA27	DDR0_DQ[61]	DDR1_DQ[45]
	BA25	DDR0_DQ[62]	DDR1_DQ[46]
	BB25	DDR0_DQ[63]	DDR1_DQ[47]
Block 7	AU27	DDR1_DQ[48]	DDR1_DQ[48]
	AT27	DDR1_DQ[49]	DDR1_DQ[49]
	AT25	DDR1_DQ[50]	DDR1_DQ[50]
	AU25	DDR1_DQ[51]	DDR1_DQ[51]
	AP27	DDR1_DQ[52]	DDR1_DQ[52]
	AN27	DDR1_DQ[53]	DDR1_DQ[53]
	AN25	DDR1_DQ[54]	DDR1_DQ[54]
	AP25	DDR1_DQ[55]	DDR1_DQ[55]
	AT22	DDR1_DQ[56]	DDR1_DQ[56]
	AU22	DDR1_DQ[57]	DDR1_DQ[57]
	AU21	DDR1_DQ[58]	DDR1_DQ[58]
	AT21	DDR1_DQ[59]	DDR1_DQ[59]
	AN22	DDR1_DQ[60]	DDR1_DQ[60]
	AP22	DDR1_DQ[61]	DDR1_DQ[61]
	AP21	DDR1_DQ[62]	DDR1_DQ[62]
	AN21	DDR1_DQ[63]	DDR1_DQ[63]

LOGIC



	PIN	Interleave	Non-Interleave
Block 4	BA38	DDR0_DQSN[4]	DDR1_DQSN[0]
	AY38	DDR0_DQSP[4]	DDR1_DQSP[0]
	AY34	DDR0_DQSN[5]	DDR1_DQSN[1]
	BA34	DDR0_DQSP[5]	DDR1_DQSP[1]
Block 5	AT38	DDR1_DQSN[4]	DDR1_DQSN[2]
	AR38	DDR1_DQSP[4]	DDR1_DQSP[2]
	AT32	DDR1_DQSN[5]	DDR1_DQSN[3]
	AR32	DDR1_DQSP[5]	DDR1_DQSP[3]
Block 6	BA30	DDR0_DQSN[6]	DDR1_DQSN[4]
	AY30	DDR0_DQSP[6]	DDR1_DQSP[4]
	AY26	DDR0_DQSN[7]	DDR1_DQSN[5]
	BA26	DDR0_DQSP[7]	DDR1_DQSP[5]
Block 7	AR25	DDR1_DQSN[6]	DDR1_DQSN[6]
	AR27	DDR1_DQSP[6]	DDR1_DQSP[6]
	AR22	DDR1_DQSN[7]	DDR1_DQSN[7]
	AR21	DDR1_DQSP[7]	DDR1_DQSP[7]

LOGIC

PIN	DDR3L	LPDDR3	DDR4
AY48	DDR1_MA[5]	DDR1_CAA[0]	DDR1_MA[5]
AP50	DDR1_MA[9]	DDR1_CAA[1]	DDR1_MA[9]
BA48	DDR1_MA[6]	DDR1_CAA[2]	DDR1_MA[6]
BB48	DDR1_MA[8]	DDR1_CAA[3]	DDR1_MA[8]
AP48	DDR1_MA[7]	DDR1_CAA[4]	DDR1_MA[7]
AP52	DDR1_BA[2]	DDR1_CAA[5]	DDR1_BG[0]
AN50	DDR1_MA[12]	DDR1_CAA[6]	DDR1_MA[12]
AN48	DDR1_MA[11]	DDR1_CAA[7]	DDR1_MA[11]
AN53	DDR1_MA[15]	DDR1_CAA[8]	DDR1_ACT#
AN52	DDR1_MA[14]	DDR1_CAA[9]	DDR1_BG[1]
BA43	DDR1_MA[13]	DDR1_CAB[0]	DDR1_MA[13]
AY43	DDR1_CAS#	DDR1_CAB[1]	DDR1_MA[15]
AY44	DDR1_WE#	DDR1_CAB[2]	DDR1_MA[14]
AW44	DDR1_RAS#	DDR1_CAB[3]	DDR1_MA[16]
BB44	DDR1_BA[0]	DDR1_CAB[4]	DDR1_BA[0]
AY47	DDR1_MA[2]	DDR1_CAB[5]	DDR1_MA[2]
BA44	DDR1_BA[1]	DDR1_CAB[6]	DDR1_BA[1]
AW46	DDR1_MA[10]	DDR1_CAB[7]	DDR1_MA[10]
AY46	DDR1_MA[1]	DDR1_CAB[8]	DDR1_MA[1]
BA46	DDR1_MA[0]	DDR1_CAB[9]	DDR1_MA[0]
BB46	DDR1_MA[3]	Not Used	DDR1_MA[3]
BA47	DDR1_MA[4]	Not Used	DDR1_MA[4]

LOGIC

<Core Design>

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Title: CPU(3/16) : DDR CHANNEL-B

Size	Document Number	Rev
A2	TS1	1

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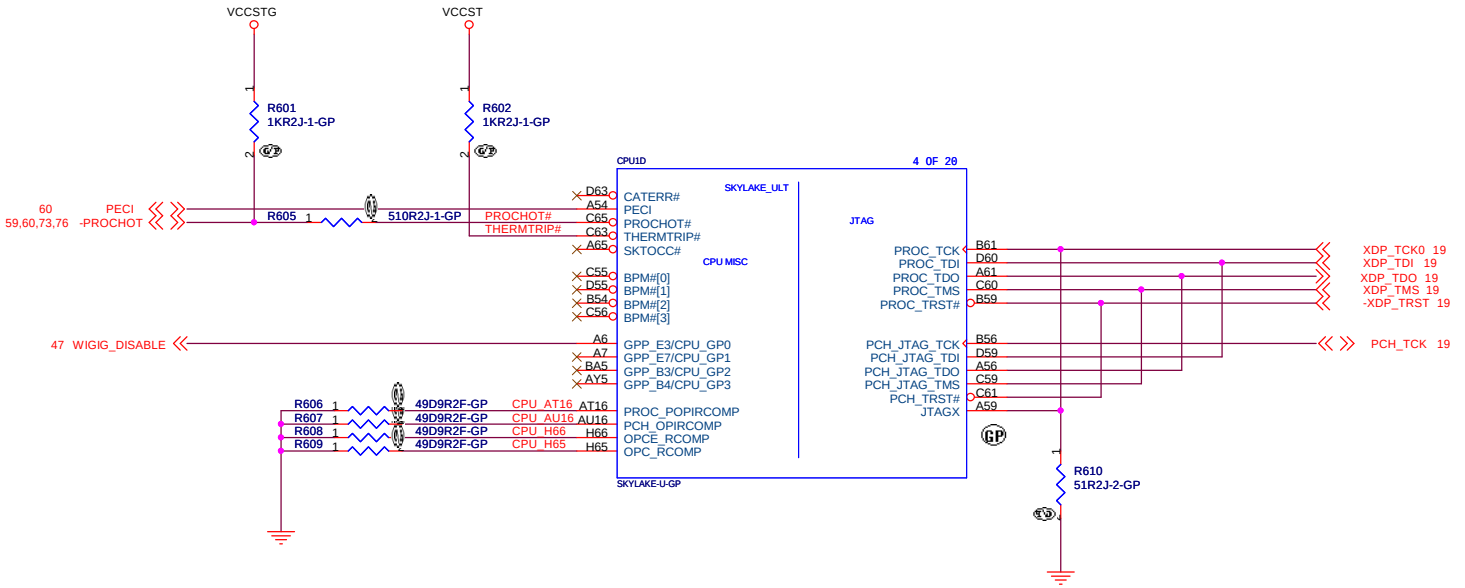

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Title: ***CPU(4/16) : MISC/JTAG***

Size	Document Number	Rev
A4	TS1	1

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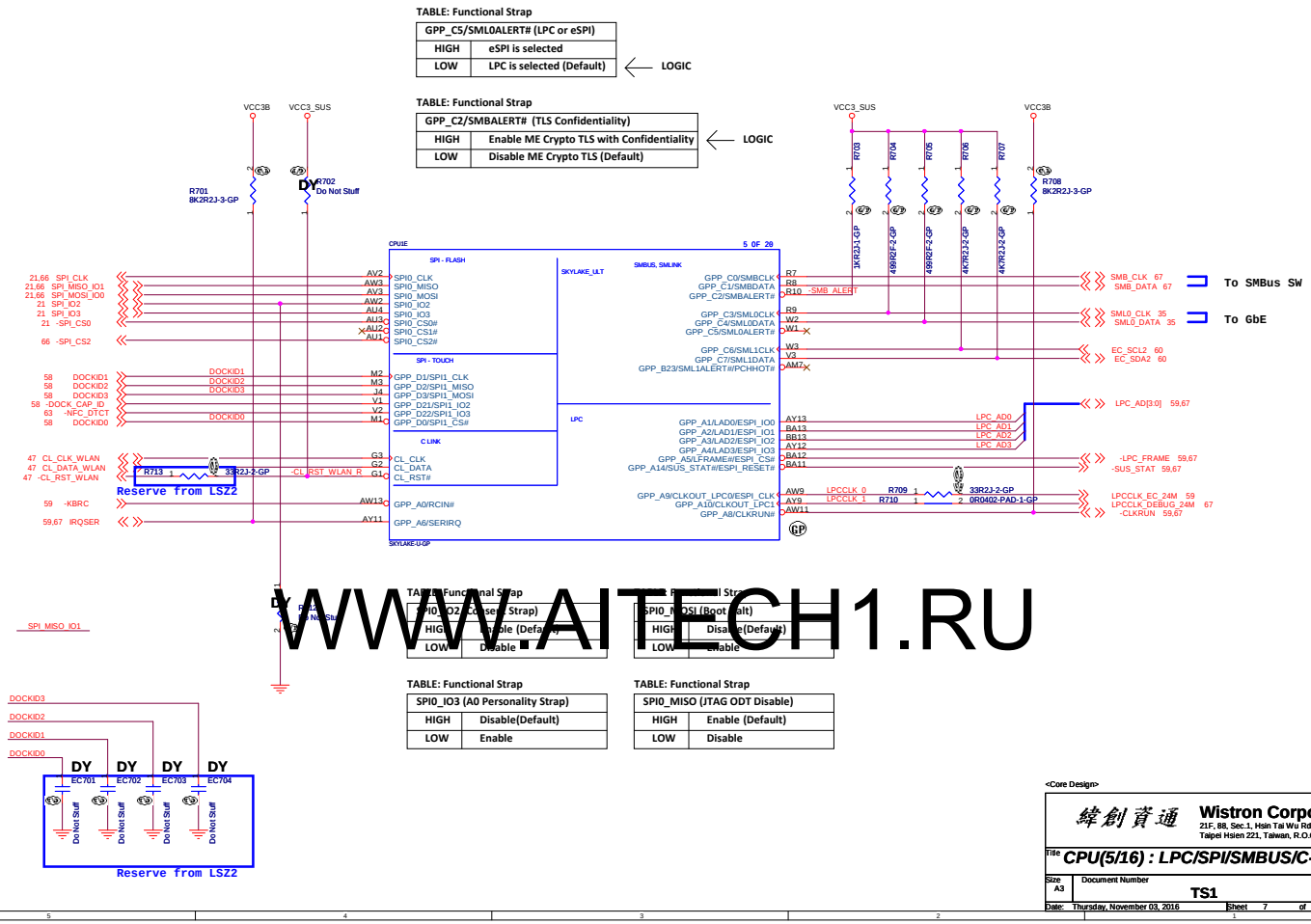

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Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU(5/16) : LPC/SPI/SMBUS/C-LINK

Size	Document Number	Rev
A3	TS1	1

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TABLE: Functional Strap

GPP_B22/GSPI1_MOSI (Boot BIOS Destination)	
HIGH	Boot BIOS from LPC
LOW	Boot BIOS from SPI (Default)

LOGIC

TABLE: Functional Strap

GPP_B18/GSPI0_MOSI (No Reboot)	
HIGH	Enable "No Reboot" Mode
LOW	Disable "No Reboot" Mode (Default)

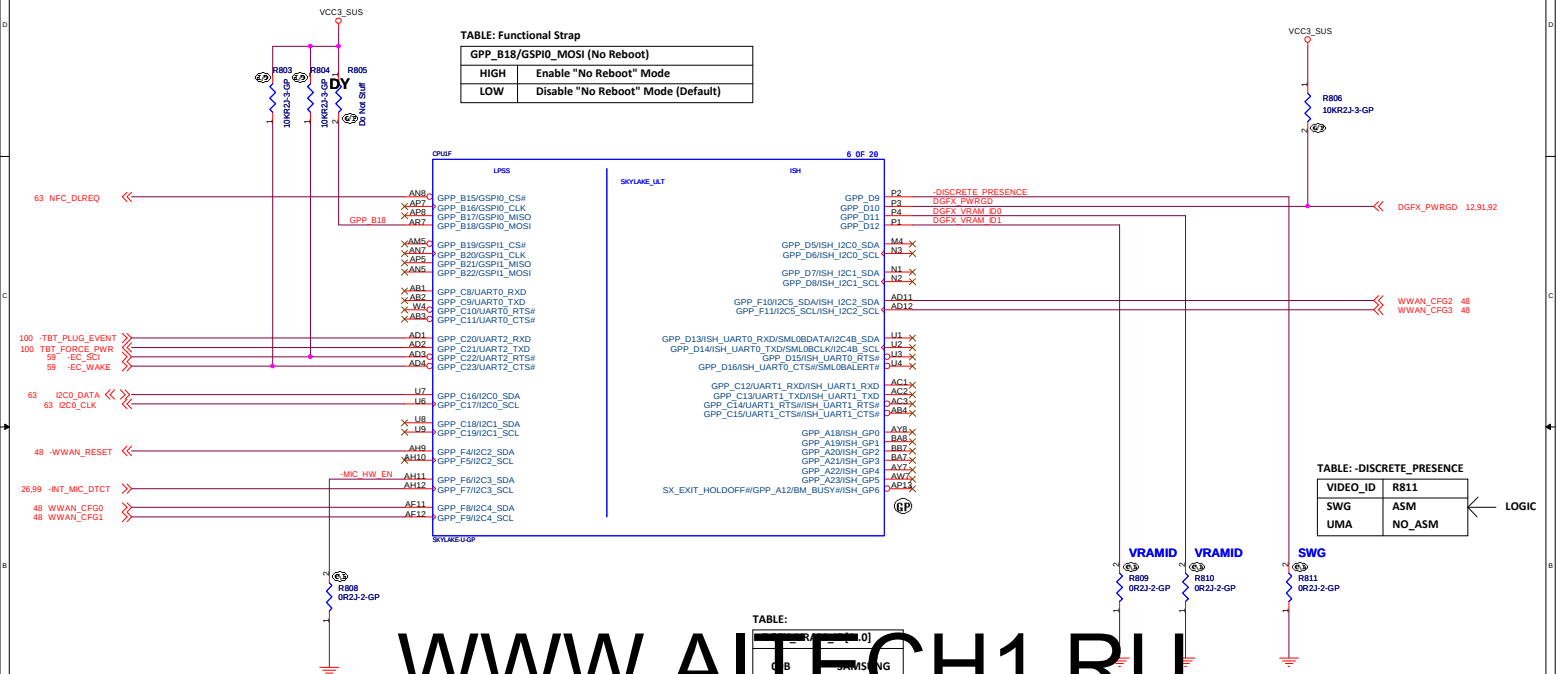

TABLE: -DISCRETE_PRESENCE

VIDEO_ID	R811
SWG	ASM
UMA	NO_ASM

LOGIC

TABLE:

[illegible]	[illegible]
08B	SAMSUNG
09B	MICRON
10B	RESERVE
11B	RESERVE

<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU(6/16) : LPSS/ISH

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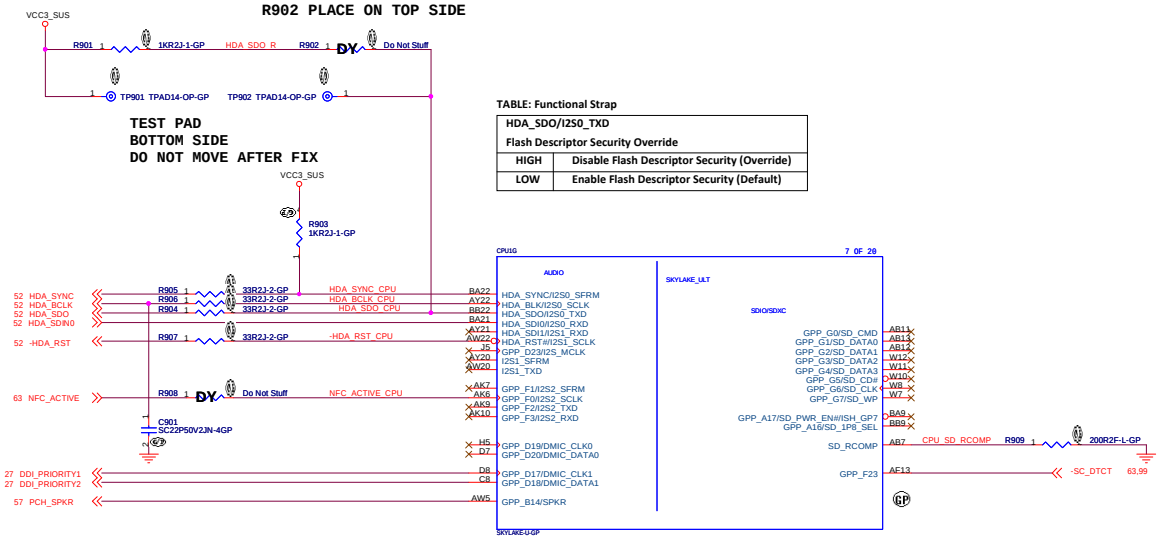

TABLE: Functional Strap

HDA_SDO/I2S0_TXD Flash Descriptor Security Override	
HIGH	Disable Flash Descriptor Security (Override)
LOW	Enable Flash Descriptor Security (Default)

TABLE: Functional Strap

GPP_B14/SPKR (Top Swap Override)	
HIGH	Enable "Top Swap" Mode
LOW	Disable "Top Swap" Mode (Default)

<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU(7/16) : AUDIO/SDXC

Size	Document Number	Rev
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Flexible I/O Configuration			
I/O	High Speed Signals	Configuration	Net Name
Port 1	USB3 1	USB3 1	USB3P0
Port 2	USB3 2/SSIC	USB3 2	USB3P1
Port 3	USB3 3	USB3 3	USB3P2
Port 4	USB3 4	USB3 4	USB3P3
Port 5	USB3 5/PCIE 1	PCIE 1 (x4)	PCIE0_L0
Port 6	USB3 6/PCIE 2	PCIE 2 (x4)	PCIE0_L1
Port 7	PCIE 3 (GbE)	PCIE 3 (x4)	PCIE0_L2
Port 8	PCIE 4 (GbE)	PCIE 4 (x4)	PCIE0_L3
Port 9	PCIE 5 (GbE)	PCIE 5 (GbE)	PCIE4
Port 10	PCIE 6	PCIE 6	PCIE5
Port 11	PCIE 7/SATA 0	PCIE 7 (x2)	PCIE6_L1
Port 12	PCIE 8/SATA 1A	GPIO STRAP	PCIE6_L0_SATA1
Port 13	PCIE 9 (GbE)	PCIE 9 (x2)	PCIE8_L1
Port 14	PCIE 10 (GbE)	PCIE 10 (x2)	PCIE8_L0
Port 15	PCIE 11/SATA 1B	PCIE 11 (x2)	PCIE10_L0
Port 16	PCIE 12/SATA 2	GPIO STRAP	PCIE10_L1_SATA2

PCIe Port Assignment	
0 (x4)	dGPU
4	Gbe PHY
5	M.2 WLAN Slot Port0
6(x2)	Optane x2 or M.2 WLAN slot Port1 x1
8(x2)	Alpine Ridge-LP
10 (x2)	Main Storage x2

SATA Port Assignment	
0	(PCIE 7)
1A	SATA SSD on WWAN slot
1B	(PCIE11)
2	SATA SSD Main Storage

USB Port Assignment	
0	USB 3.0 System Port (AOU)
1	USB 3.0 System Port (Debug)
2	Smart Card Reader
3	USB 3.0 System Port(SUB) /DOCK
4	IR camera
5	WWAN Card
6	M.2 WLAN Slot for BT
7	USB Camera
8	Fingerprint Reader
9	Touch Panel

USB 3.0 Port Assignment	
0	USB 3.0 System Port (AOU)
1	USB 3.0 System Port
2	Media Card controller
3	USB 3.0 System Port(SUB) /DOCK
4	(PCIE 1)
5	(PCIE 2)

Pericom PI3PCIE3212ZBE 071.33212.0003
NXP CBTL02043ABQ 071.02043.0003
TOSHIBA TC7PCI3212MT 071.73212.0003

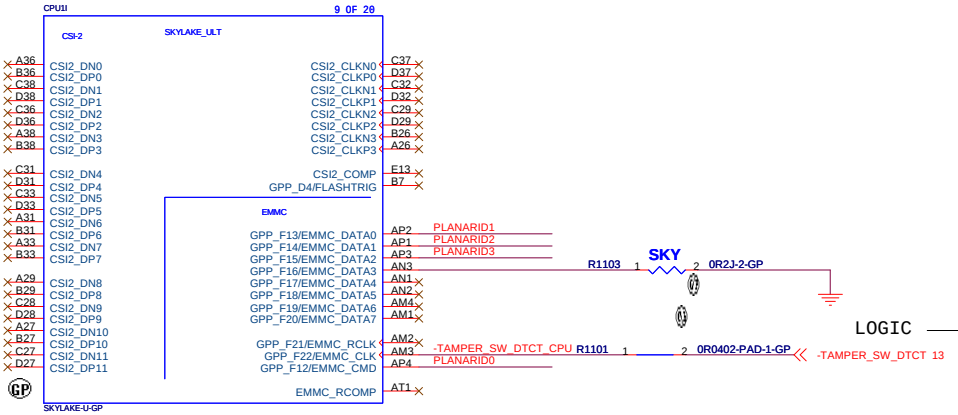
Pericom PI3USB102ZME 73.3US10.D03
NXP NX3DV42GU 73.00342.003

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

CPU(8/16) : PCIE/USB/SATA

Size: A2 | Document Number: TS1 | Rev: 1

Date: Thursday, November 03, 2016 | Sheet 30 of 100



LOGIC

TABLE

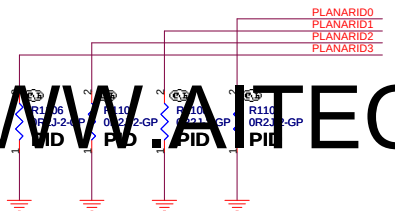
LEVEL	PLANAR ID			
	3	2	1	0
	R1106	R1107	R1108	R1109
1	NA	NA	NA	NA
0	ASM	ASM	ASM	ASM

TABLE

LEVEL	PLANARID[3..0]		
	UMA	GeForce (N16S-GTR)	Quadro(N17M-Q1)
SDV	0000B	0001B	0010B
FVT1/FVT2	0011B	0100B	0101B
SIT/SIT2	0110B	0111B	1000B
SVT	1001B	1010B	1011B
MP	1100B	1101B	1110B

TABLE

	R1103
Kabylake	DY
Skylake	ASM



<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

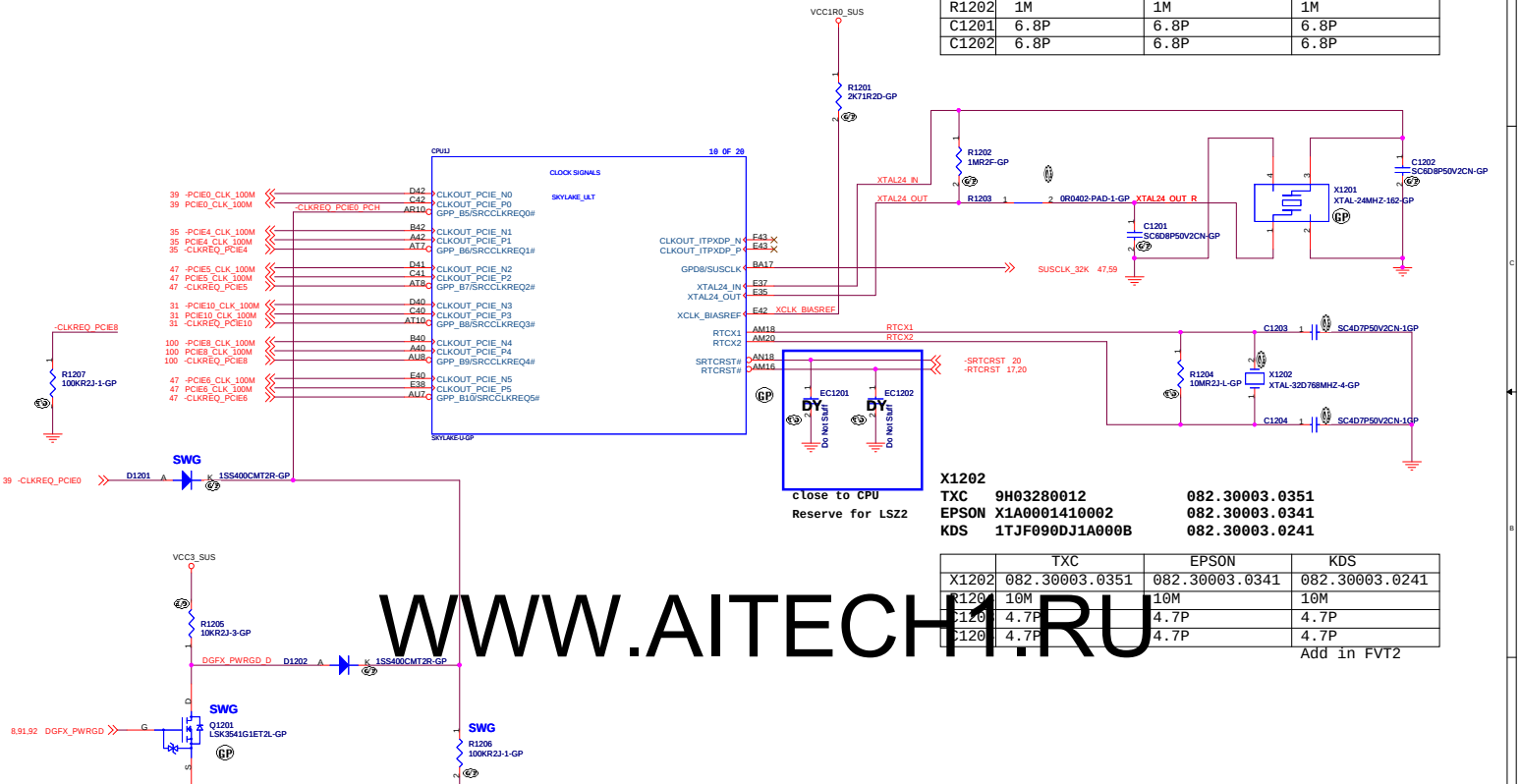
Title: **CPU(9/16) : CSI-2/EMMC**

Size	Document Number	Rev
Custom	TS1	1

Date: Thursday, November 03, 2016 Sheet 11 of 103

X1201
TXC 7R24080003
EPSON Q22FA1280055800
KDS 1ZZHAE24000CC0G

	TXC	EPSON	KDS
X1201	082.30006.0341	082.30006.0321	082.30006.0301
R1202	1M	1M	1M
C1201	6.8P	6.8P	6.8P
C1202	6.8P	6.8P	6.8P



X1202
TXC 9H03280012 082.30003.0351
EPSON X1A0001410002 082.30003.0341
KDS 1TJF090DJ1A000B 082.30003.0241

close to CPU
Reserve for LSZ2

	TXC	EPSON	KDS
X1202	082.30003.0351	082.30003.0341	082.30003.0241
R1201	10M	10M	10M
C1201	4.7P	4.7P	4.7P
C1202	4.7P	4.7P	4.7P

Add in FVT2

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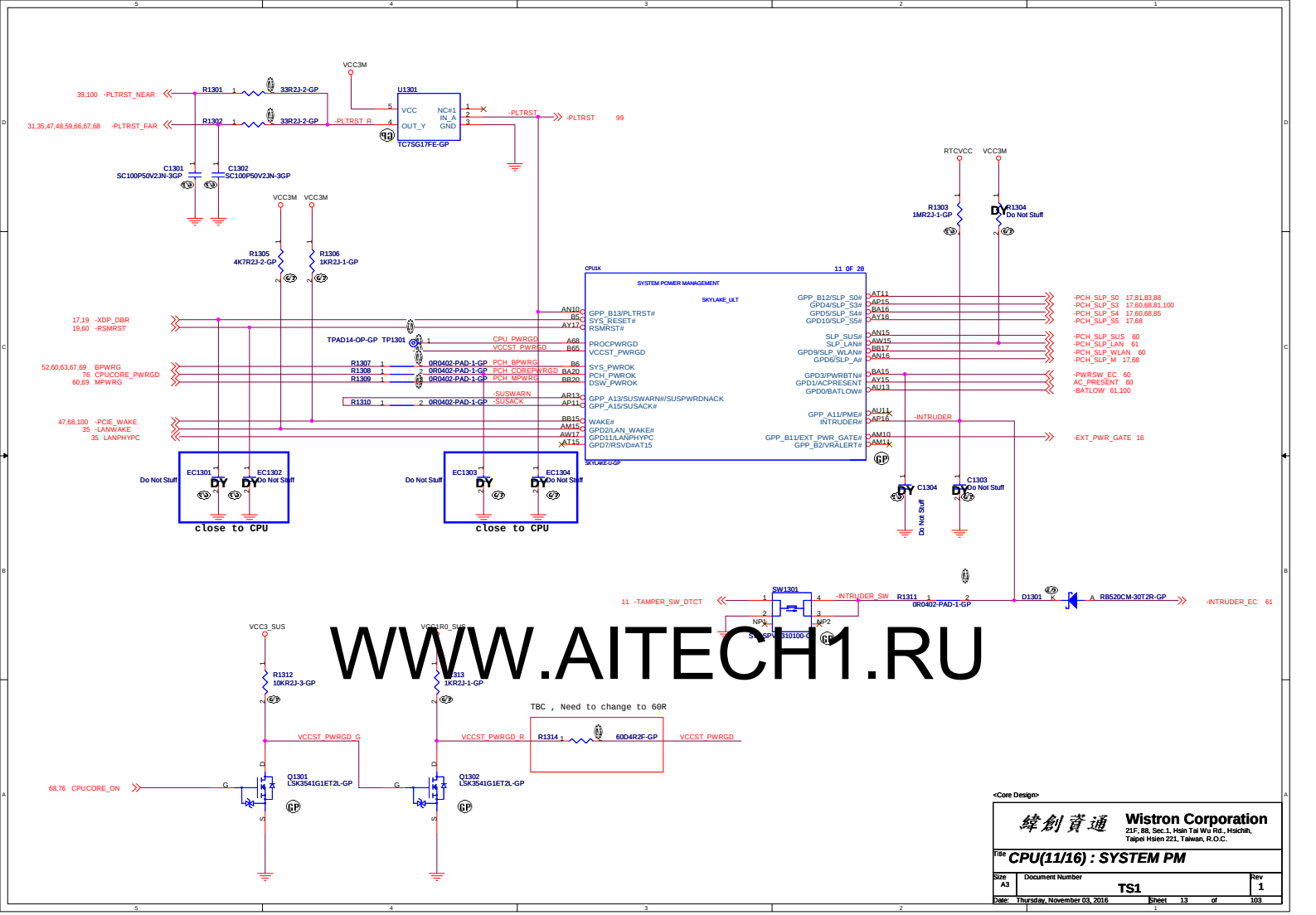
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU(10/16) : CLOCK SIGNALS

Size	Document Number	Rev
A3	TS1	1

Date: Thursday, November 03, 2016 Sheet 12 of 103



<Core Design>

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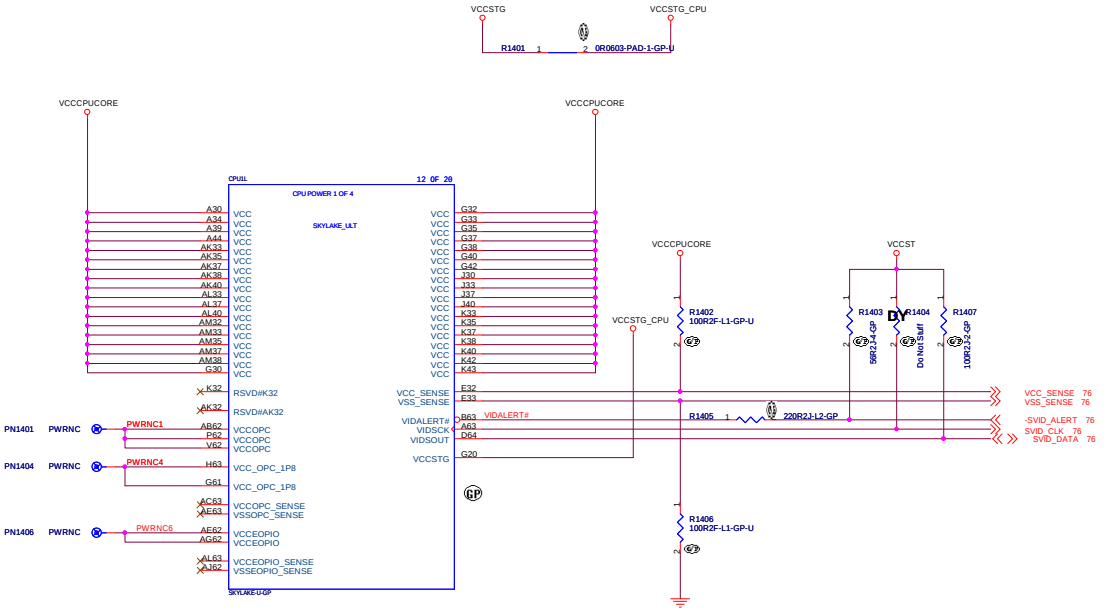
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU(11/16) : SYSTEM PM

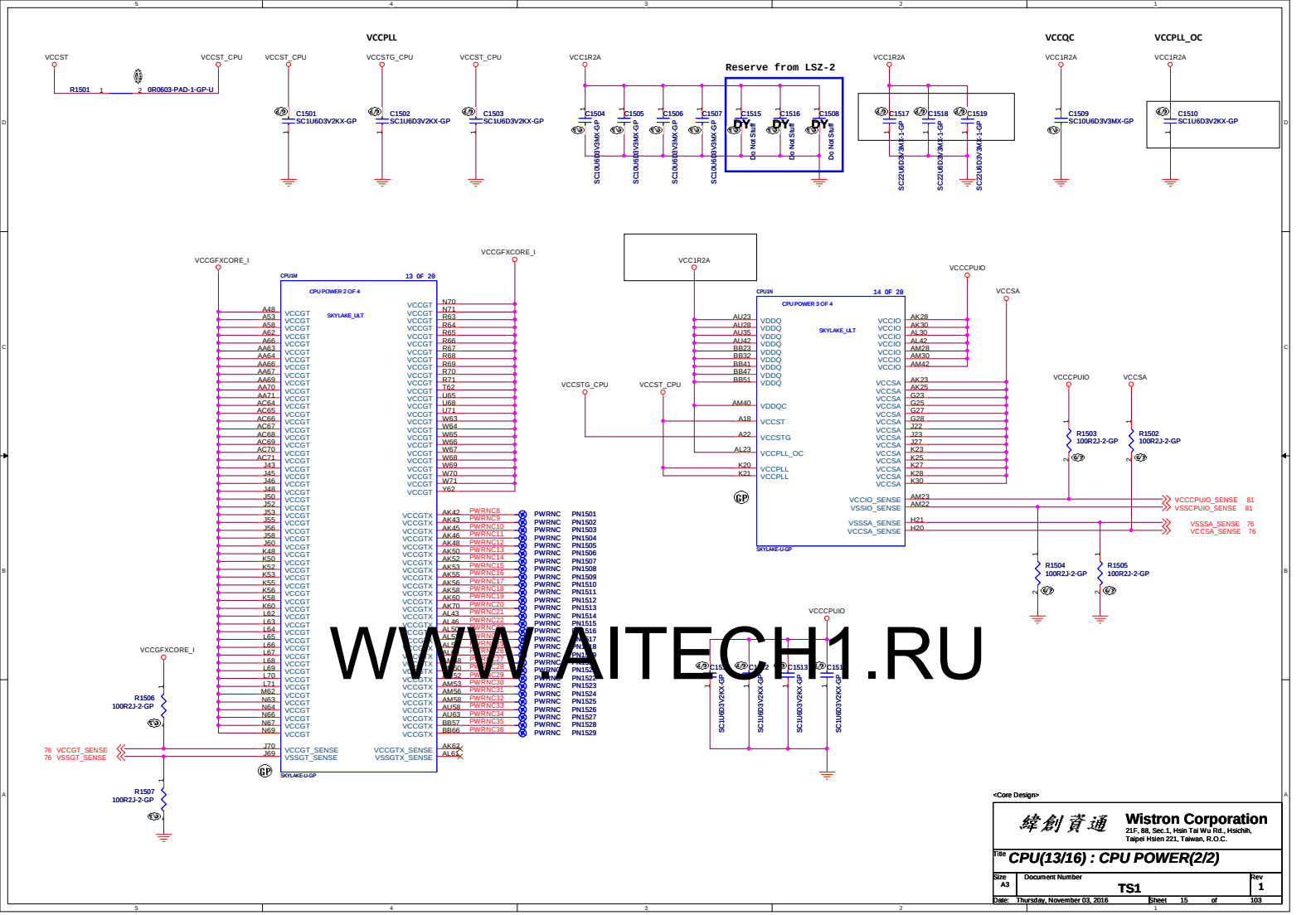
Size	Document Number	Rev
A3	TS1	1

Date: Thursday, November 03, 2016 Sheet 13 of 103



<Core Design>

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title: CPU(12/16) : CPU POWER(1/2)		
Size: A3	Document Number: TS1	Rev: 1
Date: Thursday, November 03, 2016	Sheet 14 of 103	



<Core Design>

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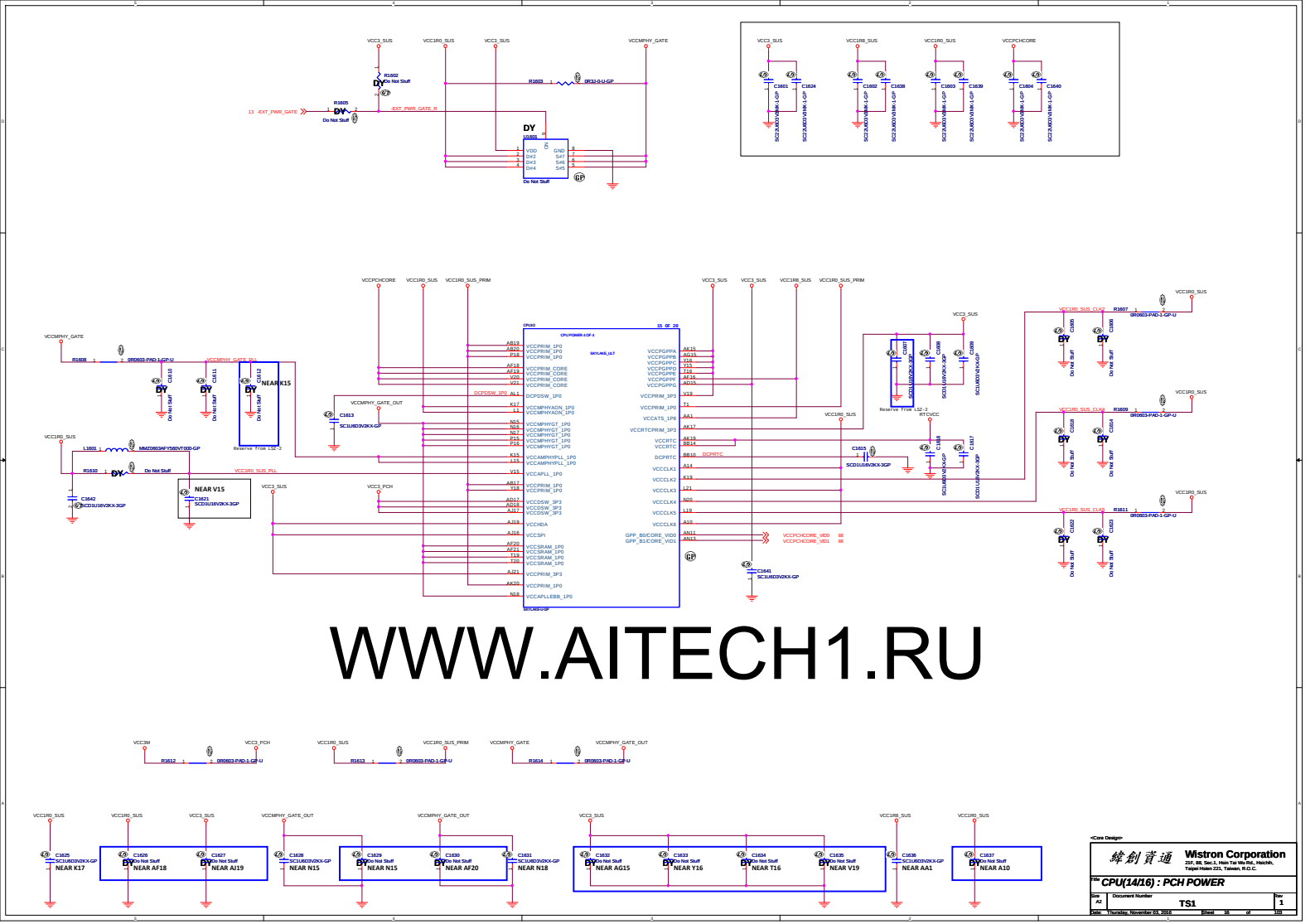
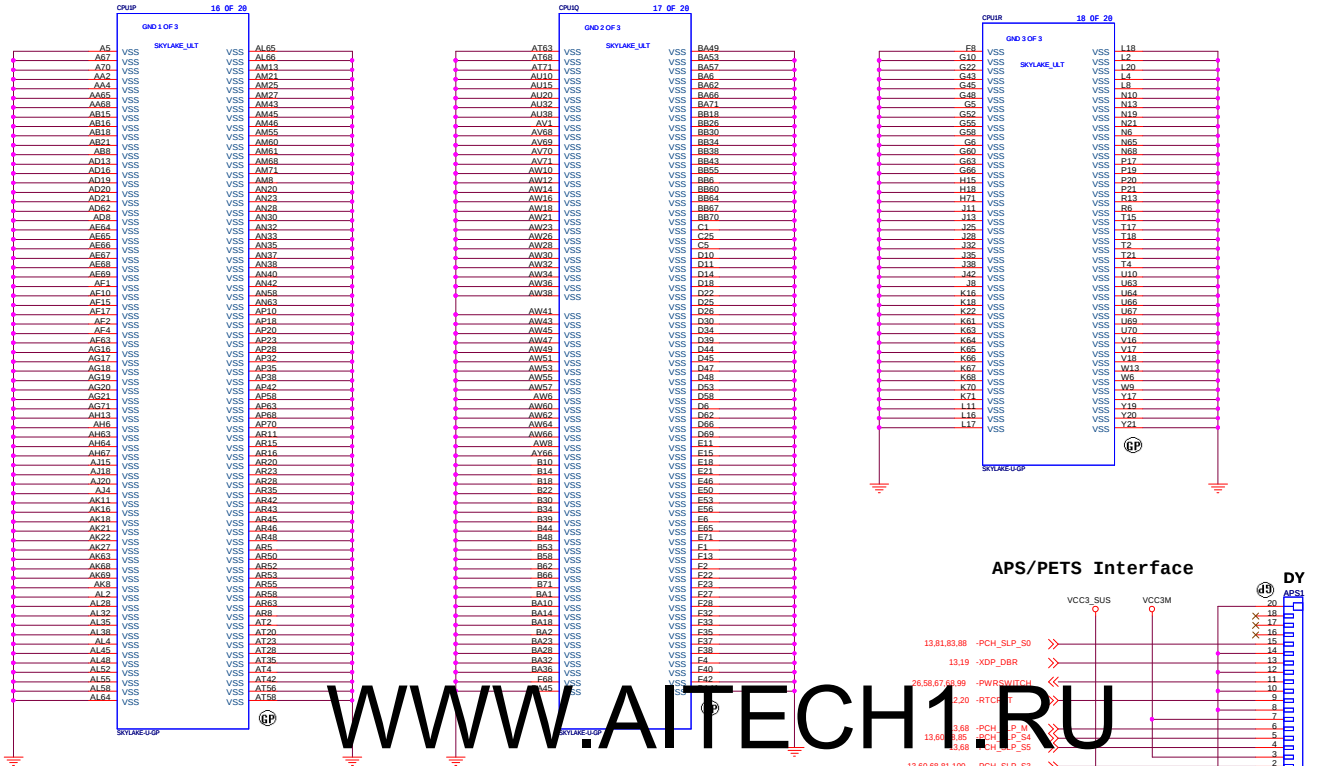
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU(13/16) : CPU POWER(2/2)

Size	Document Number	Rev
A3	TS1	1

Date: Thursday, November 03, 2016 Sheet 15 of 103





<Core Design>

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

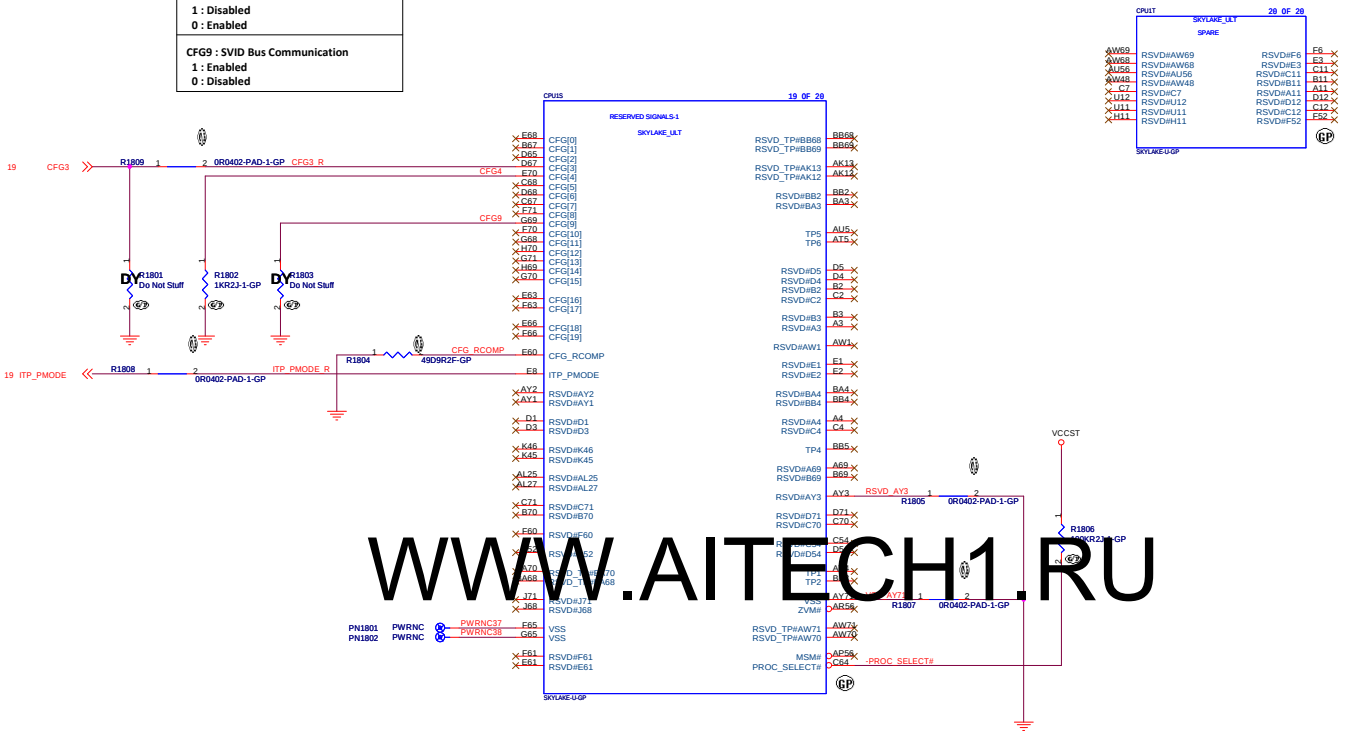
Title: CPU(15/16) : GND

Size	Document Number	Rev
A3	TS1	1

Date: Thursday, November 03, 2016 Sheet 17 of 103

TABLE

CFG0 : Stall Reset Sequence **after PCU PLL Lock until de-asserted** **1 : No Stall** **0 : Stall**
CFG3 : MSR Privacy Bit Feature **1 : MSR (C80h) bit[0] setting** **0 : MSR (C80h) bit[0] overridden**
CFG4 : eDP Enable **1 : Disabled** **0 : Enabled**
CFG9 : SVID Bus Communication **1 : Enabled** **0 : Disabled**



<Core Design>

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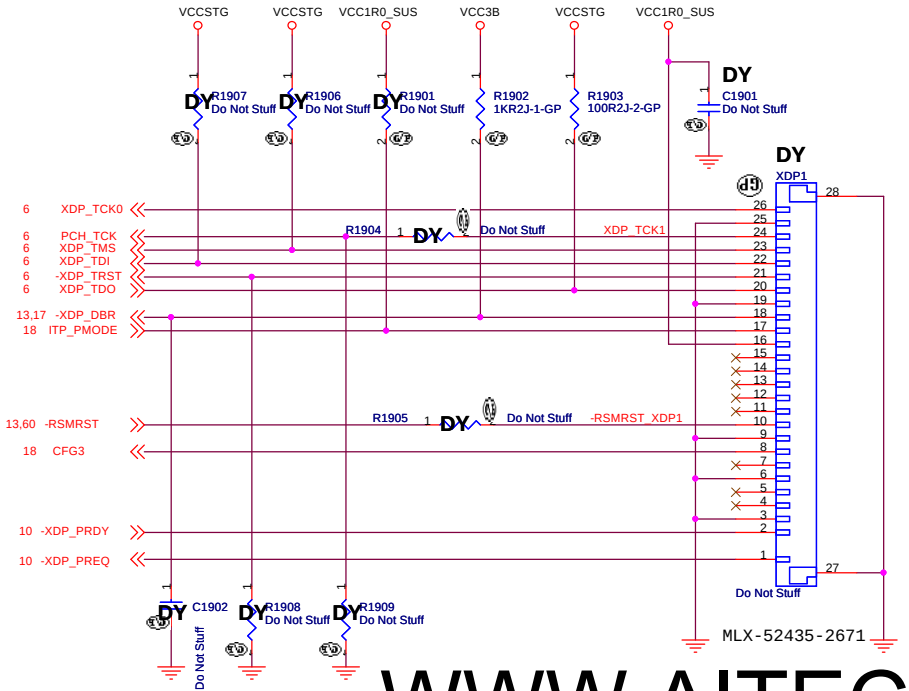
Taipei Hsien 221, Taiwan, R.O.C.

Title: **CPU(16/16) : CFG/RESERVED**

Size	Document Number	Rev
A3	TS1	1

Date: Thursday, November 03, 2016 Sheet 18 of 103



TABLE

Logic	Ref Des	Merged	DCI 2.0
Page 7	R712	ASM	NO_ASM
Page 18	R1801	ASM	NO_ASM
Page 19	XDP1	ASM	NO_ASM
	C1901	ASM	NO_ASM
	R1901	ASM	NO_ASM
	R1902	ASM	ASM
	R1903	ASM	ASM
	R1904	ASM	NO_ASM
	R1905	ASM	NO_ASM

LOGIC

<Core Design>

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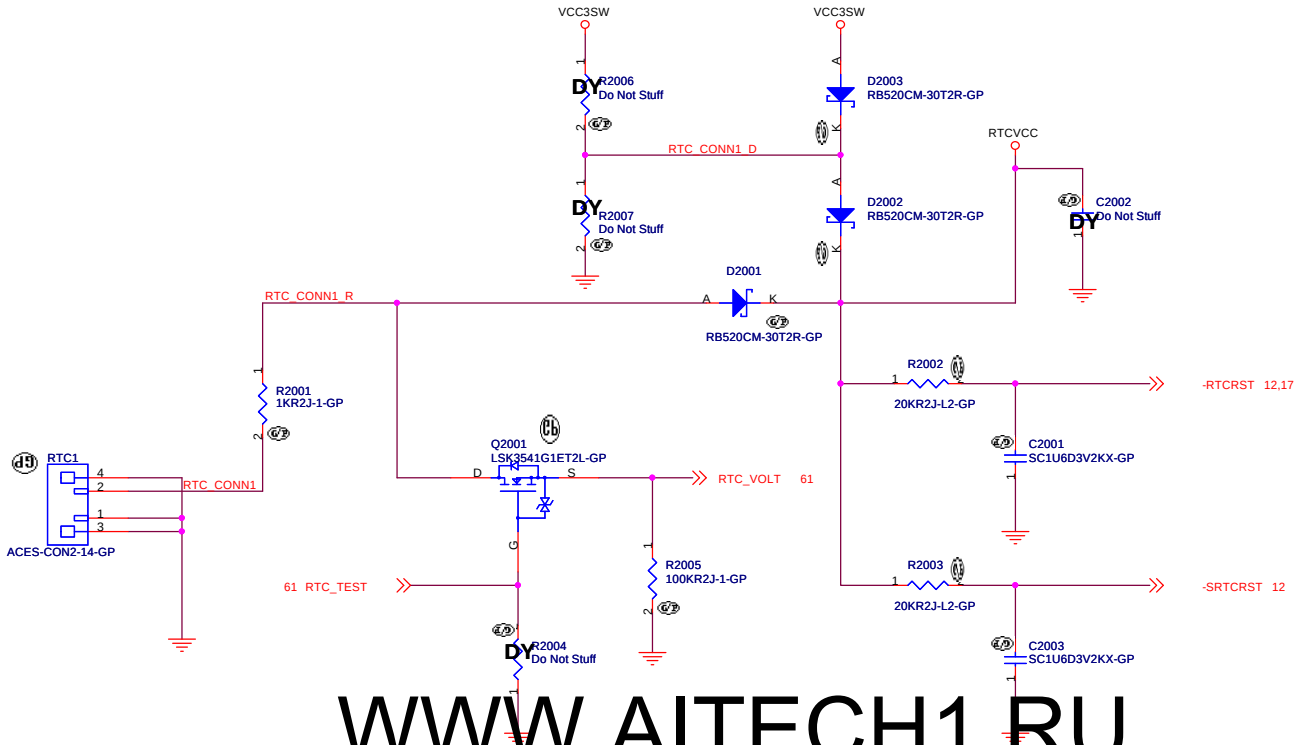
Title **XDP CONNECTOR**

Size	Document Number	Rev
A4	TS1	1

Date: Thursday, November 03, 2016 Sheet 19 of 103



for test point, page 91

RTC_CONN1 → RTC_CONN1 99

<Core Design>

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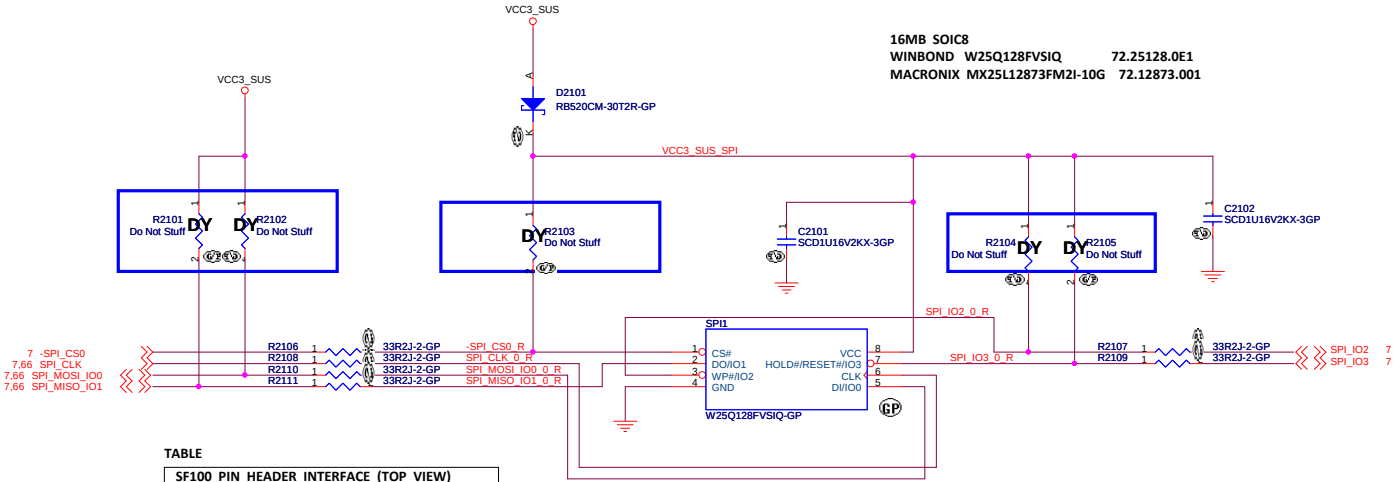
Title: RTC BATTERY

Size	Document Number	Rev
A4	TS1	1

Date: Thursday, November 03, 2016 Sheet 20 of 103



16MB SOIC8
WINBOND W25Q128FVSIQ 72.25128.0E1
MACRONIX MX25L12873FM2I-10G 72.12873.001

TABLE

SF100 PIN HEADER INTERFACE (TOP VIEW)					
1	VCC	D2101.K	GND	GND	2
3	CS#	R2104.2	R2106.2	CLK	4
5	MISO	R2109.2	R2108.2	MOSI	6
7	(KEY)	N/A	N/A	(RESET)	8

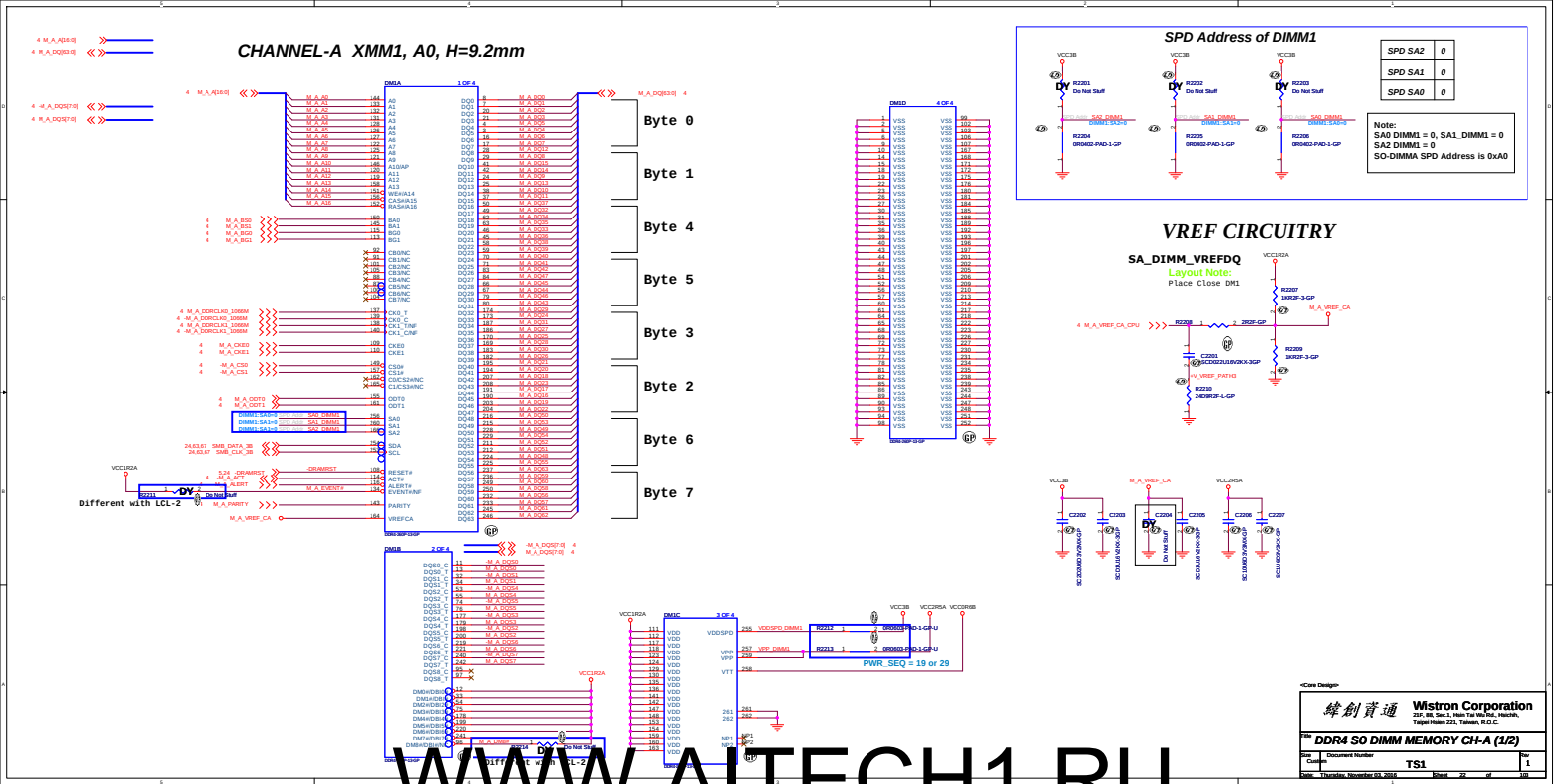
<Core Design>

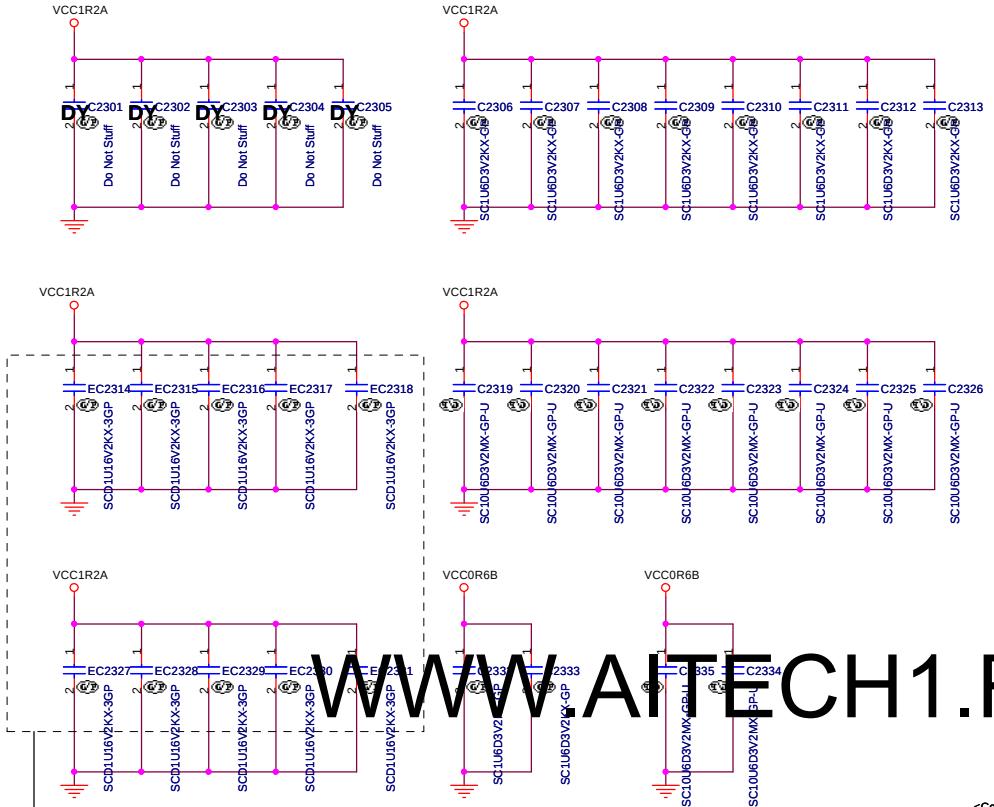
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: SPI FLASH

Size	Document Number	Rev
Custom	TS1	1

Date: Thursday, November 03, 2016 Sheet 21 of 103





ASM from EMI request.

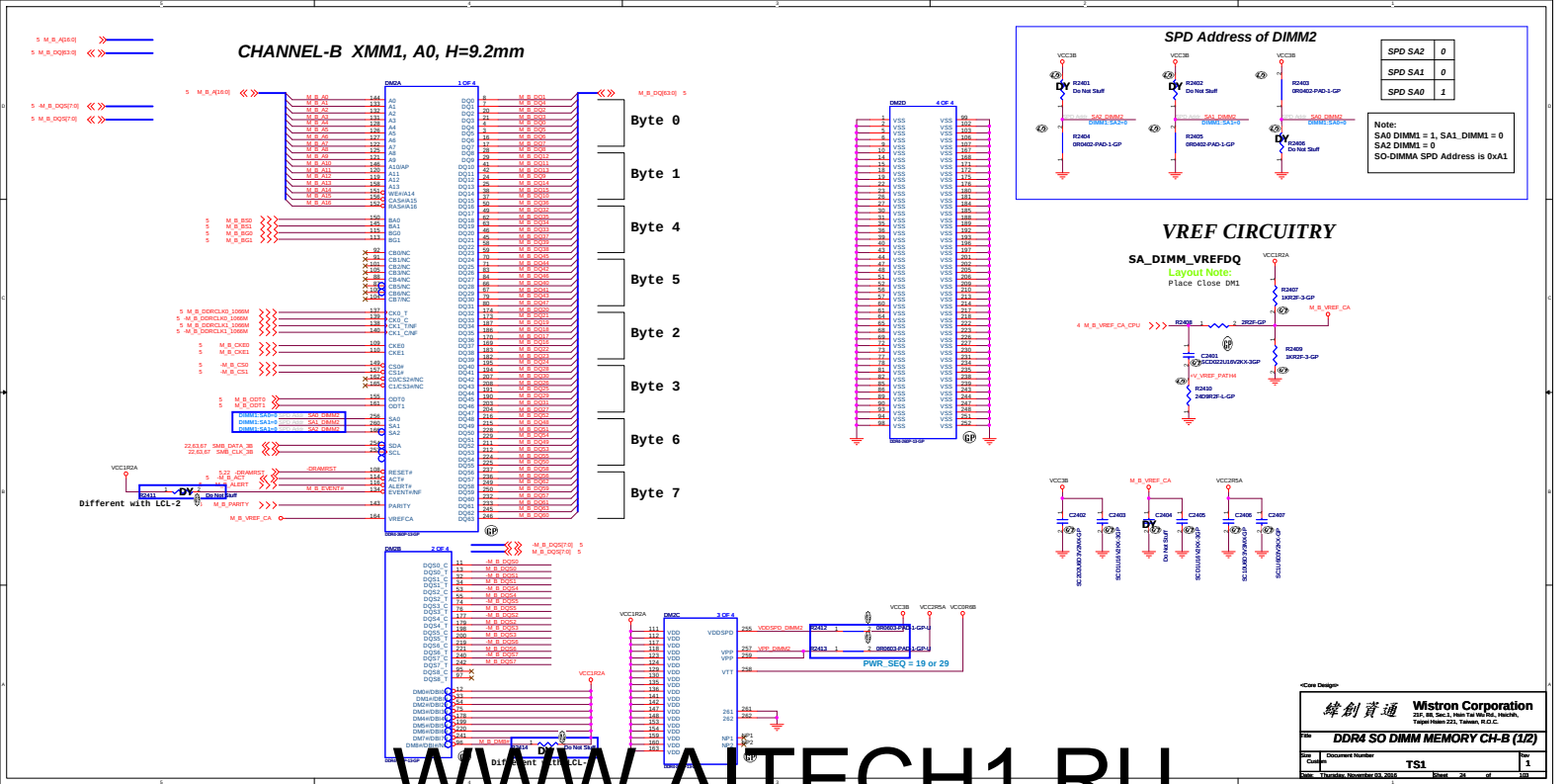
<Core Design>

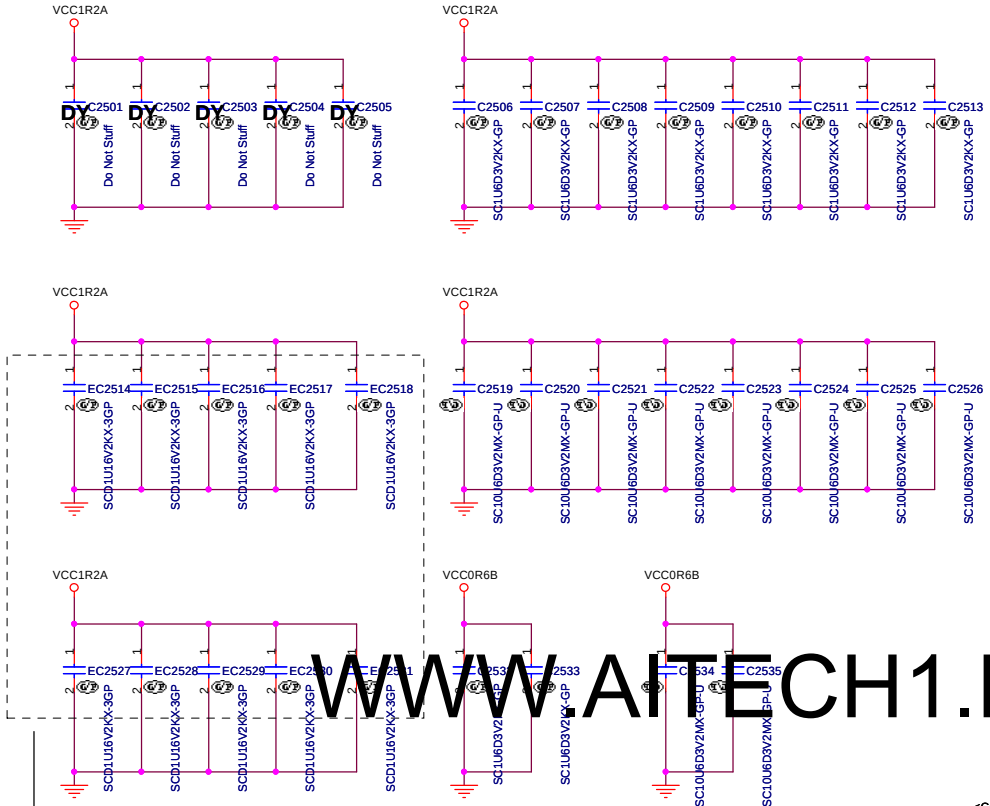
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DDR4 SO DIMM MEMORY CH-A (2/2)

Size	Document Number	Rev
A4	TS1	1

Date: Thursday, November 03, 2016 Sheet 23 of 103





ASM from EMI request.

<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DDR4 SO DIMM MEMORY CH-B (2/2)

Size	Document Number	Rev
A4	TS1	1

Date: Thursday, November 03, 2016 Sheet 25 of 103

LCD CONN

Q2601		
Vendor	Venor PN	Wistron PN
Rohm	RF4E070GN (1st source)	084.4E070.0037
Fairchild	FDMA7672 (2nd source)	084.07672.M001

0.9A

1.2A

LCD CONNECTOR

TABLE:

TP_EN	
HIGH	Enable Touch Panel
LOW	Disable Touch Panel

for test point, page 91

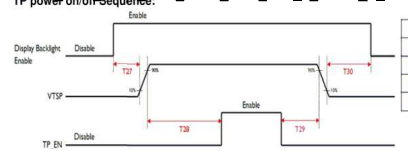
Change for HL DY

Change for HL

Power BTN

Near LCD CONN: LCD1 (P.91)

TP power on/off Sequence:



	Min	Max
T27	10ms	-
T28	20ms	-
T29	2ms	-
T30	100ms	-

<Core Design>

Wistron Corporation
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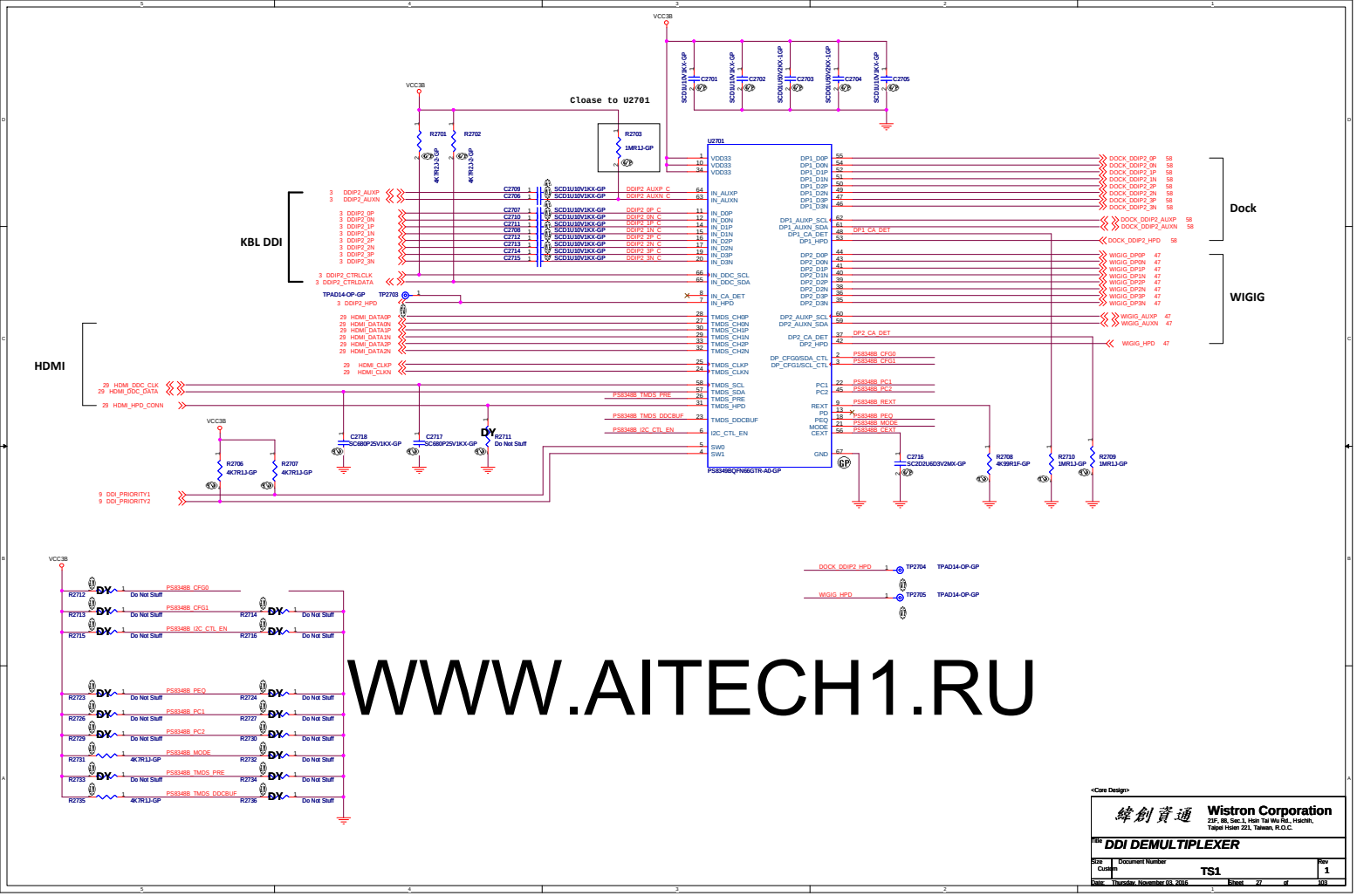
Taipei Hsien 221, Taiwan, R.O.C.

Title: LCD/LID/MIC/CAMERA/PWR SW

Size	Document Number	Rev
A2	TS1	1

Date: Thursday, November 03, 2016 Sheet 26 of 100



Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C

Title: DDI DEMULTIPLEXER

Size	Document Number	Rev
Custom	TS1	1

Date: Thursday, November 03, 2016 Sheet 27 of 103

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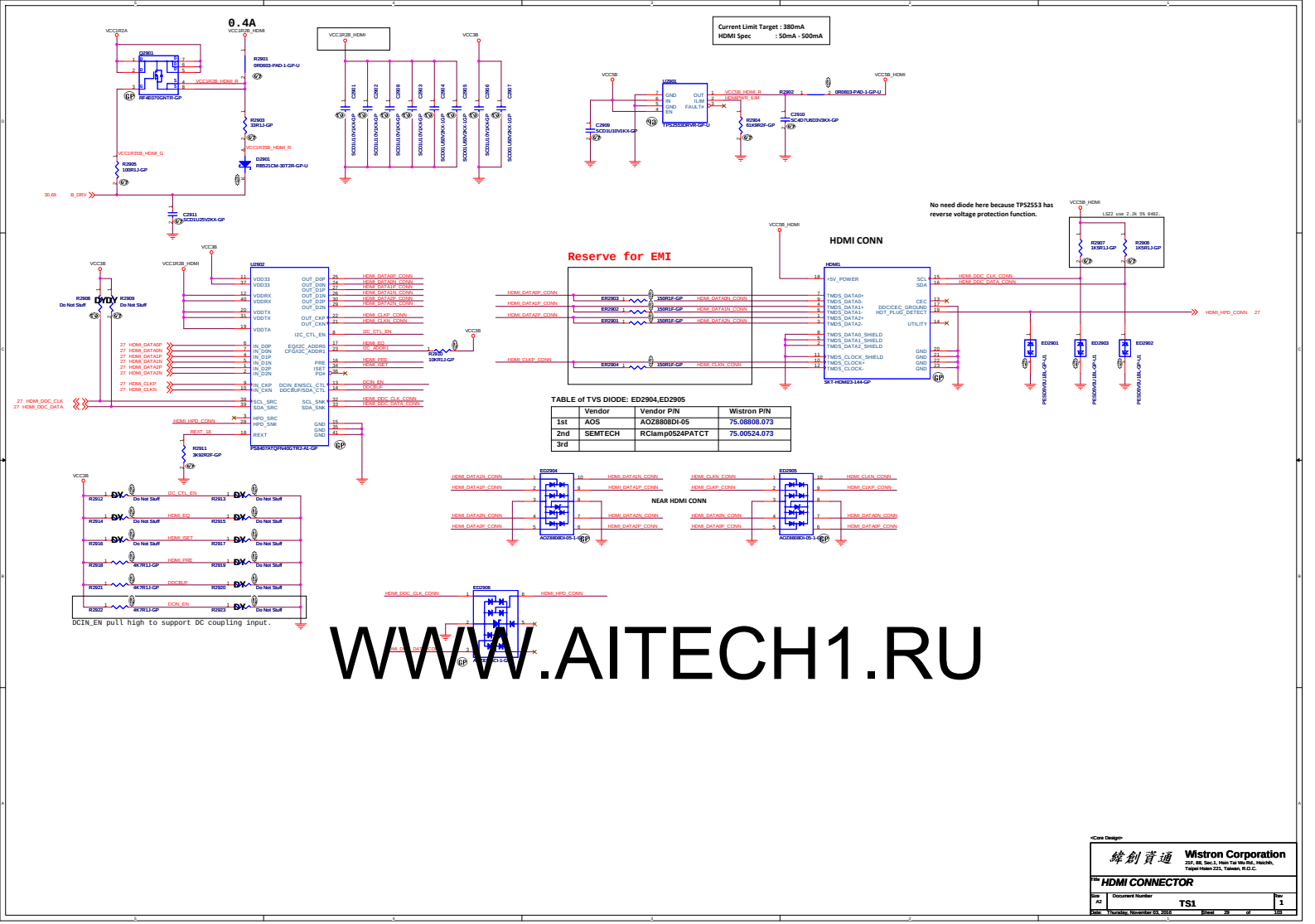
WWW.AITECH1.RU

<Core Design>

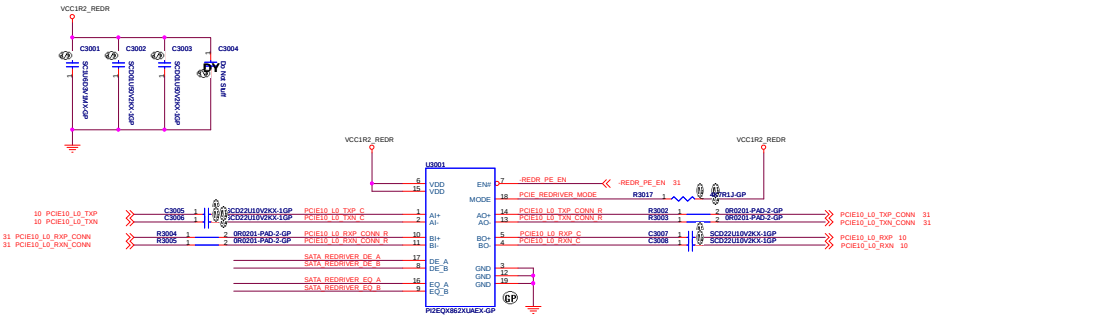
緯創資通

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

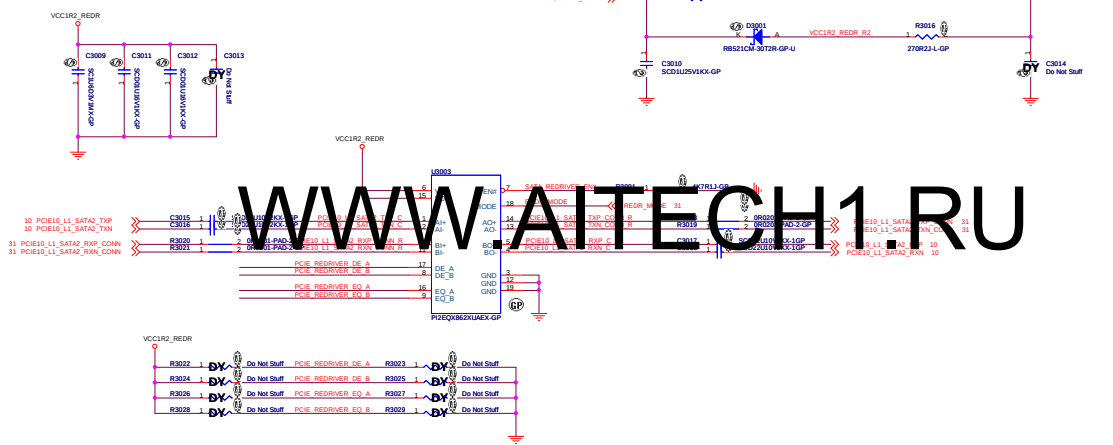
Title: ***BLANK***		
Size: A	Document Number: **TS1**	Rev: **1**
Date: Thursday, November 03, 2016	Sheet 28 of 103	

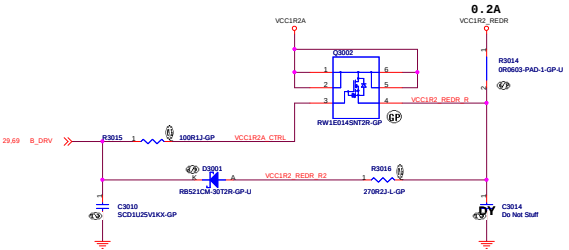

0.4A
Current Limit Target : 380mA
HDMI Spec : 50mA - 500mA
No need diode here because TPS2553 has reverse voltage protection function.
Reserve for EMI
HDMI CONN
TABLE of TVS DIODE: ED2904,ED2905
Vendor | Vendor P/N | Wistron P/N
1st | AOS | AOZ8808DI-05 | 75.08808.073
2nd | SEMTECH | RClamp0524PATCT | 75.00524.073
3rd
NEAR HDMI CONN
DCIN_EN pull high to support DC coupling input.
WWW.AITECH1.RU
Wistron Corporation
HDMI CONNECTOR
TS1

FOR PCIE ONLY



FOR SATA/PCIE





<Core Design>

Wistron Corporation
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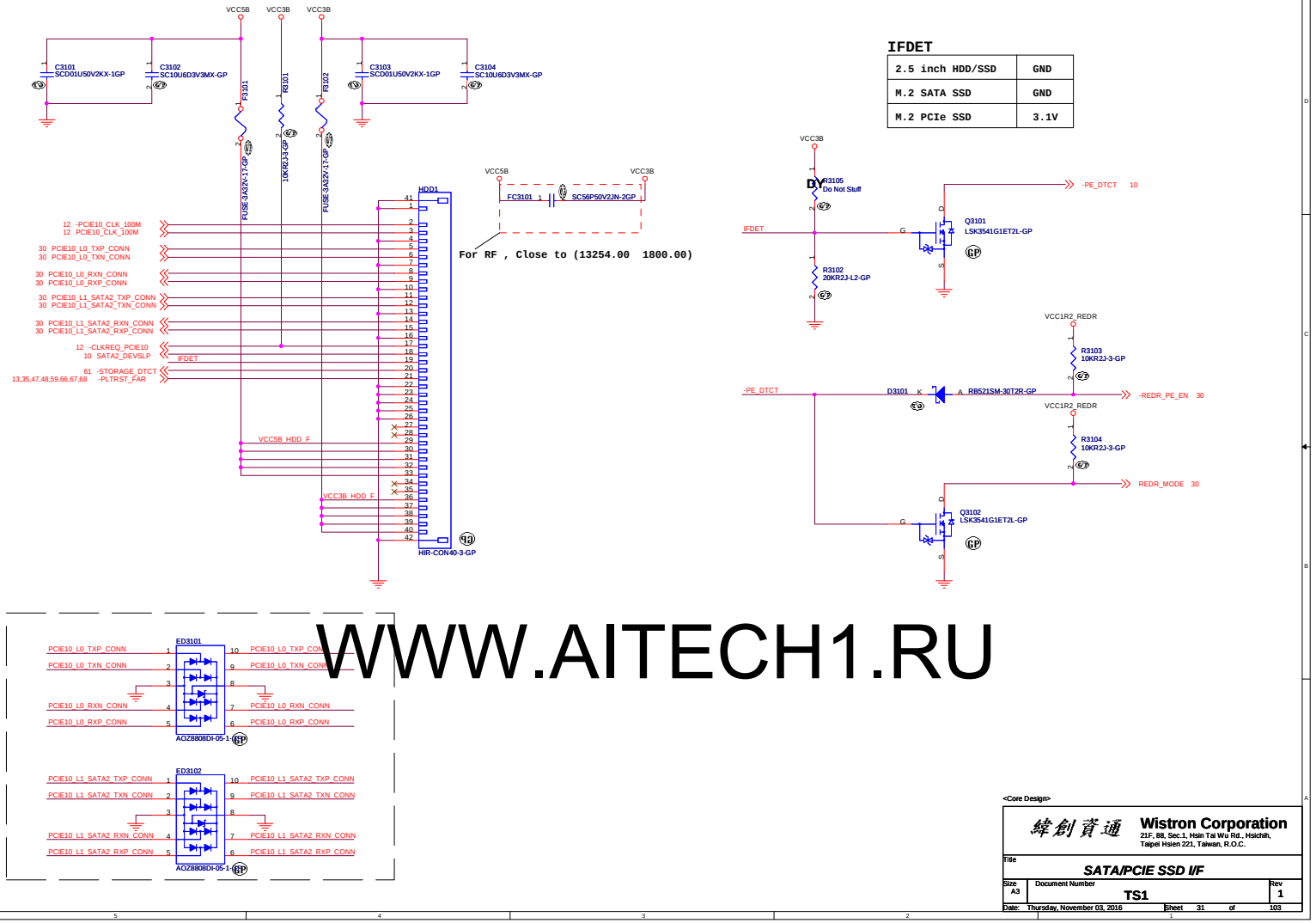
Taipei Hsien 221, Taiwan, R.O.C.

Title: STORAGE I/F REDRIVER

Size	Document Number	Rev
C	TS1	1

Date: Thursday, November 03, 2016 Sheet 30 of 103



<Core Design>

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: SATA/PCIE SSD I/F

Size	Document Number	Rev
A3	TS1	1

Date: Thursday, November 03, 2016 Sheet 31 of 103

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<Core Design>

緯創資通

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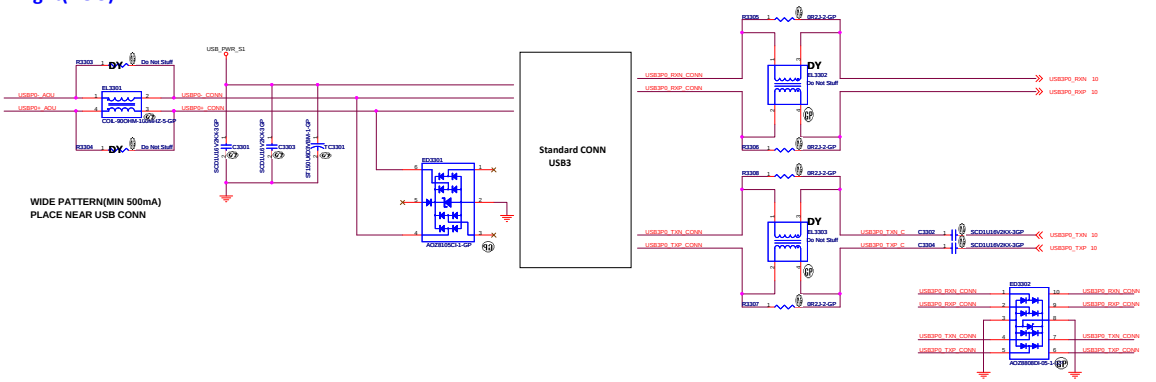
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***BLANK***		
Size: A	Document Number: **TS1**	Rev: **1**
Date: Thursday, November 03, 2016	Sheet 32 of 103	

Port1: Right(AOU)



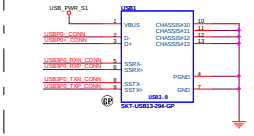
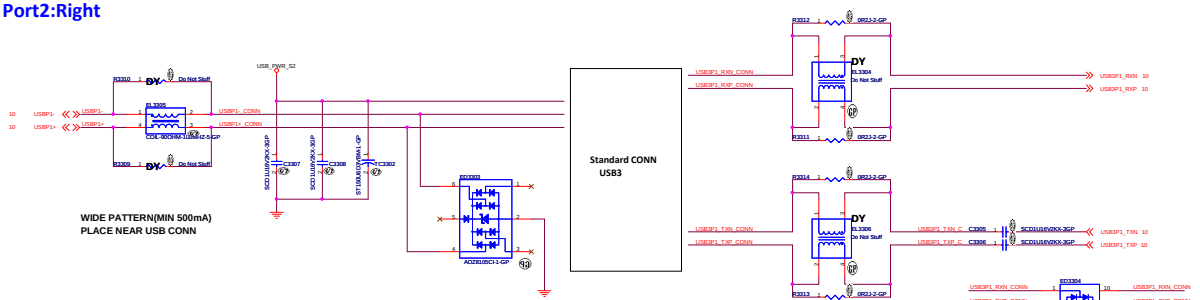


TABLE of TVS DIODE: ED3302

	Vendor	Vendor P/N	Wistron P/N
1st	AOS	AOZ8808DI-05	75.08808.073
2nd	SEMTECH	RClamp0524PATCT	75.00524.073
3rd			

Port2:Right



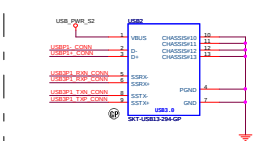
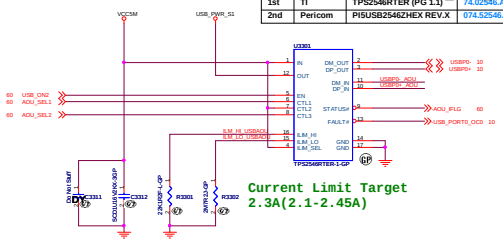


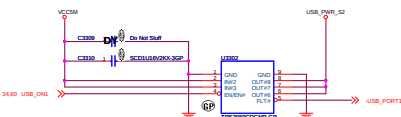
TABLE of TVS DIODE: ED3304

	Vendor	Vendor P/N	Wistron P/N
1st	AOS	AOZ8808DI-05	75.08808.073
2nd	SEMTECH	RClamp0524PATCT	75.00524.073
3rd			

TABLE of AOU port: U3301

	Vendor	Vendor P/N	Wistron P/N
1st	TI	TPS2546RTER (PG 1.1)	74.02546.A73
2nd	Pericom	PI5USB2546ZHEX REV.X	074.52546.0A73





FOR ON BOARD SINGLE USB 3.0 CONNECTOR

Continous Current Limit 1.5A

TABLE of USB 3.0 port: U3302

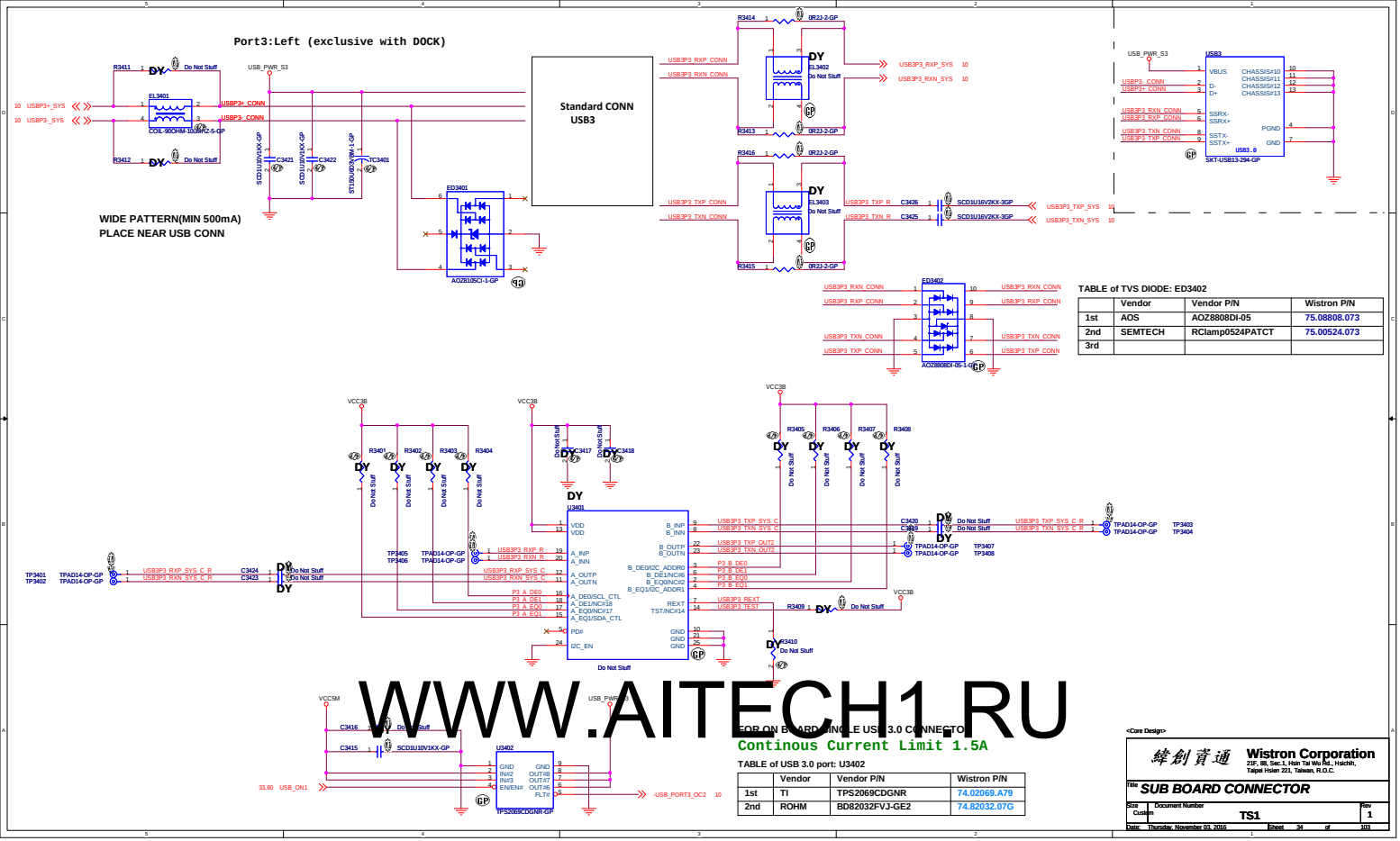
	Vendor	Vendor P/N	Wistron P/N
1st	TI	TPS2069CDGNR	74.02069.A79
2nd	ROHM	BD82032FVJ-GE2	74.82032.07G

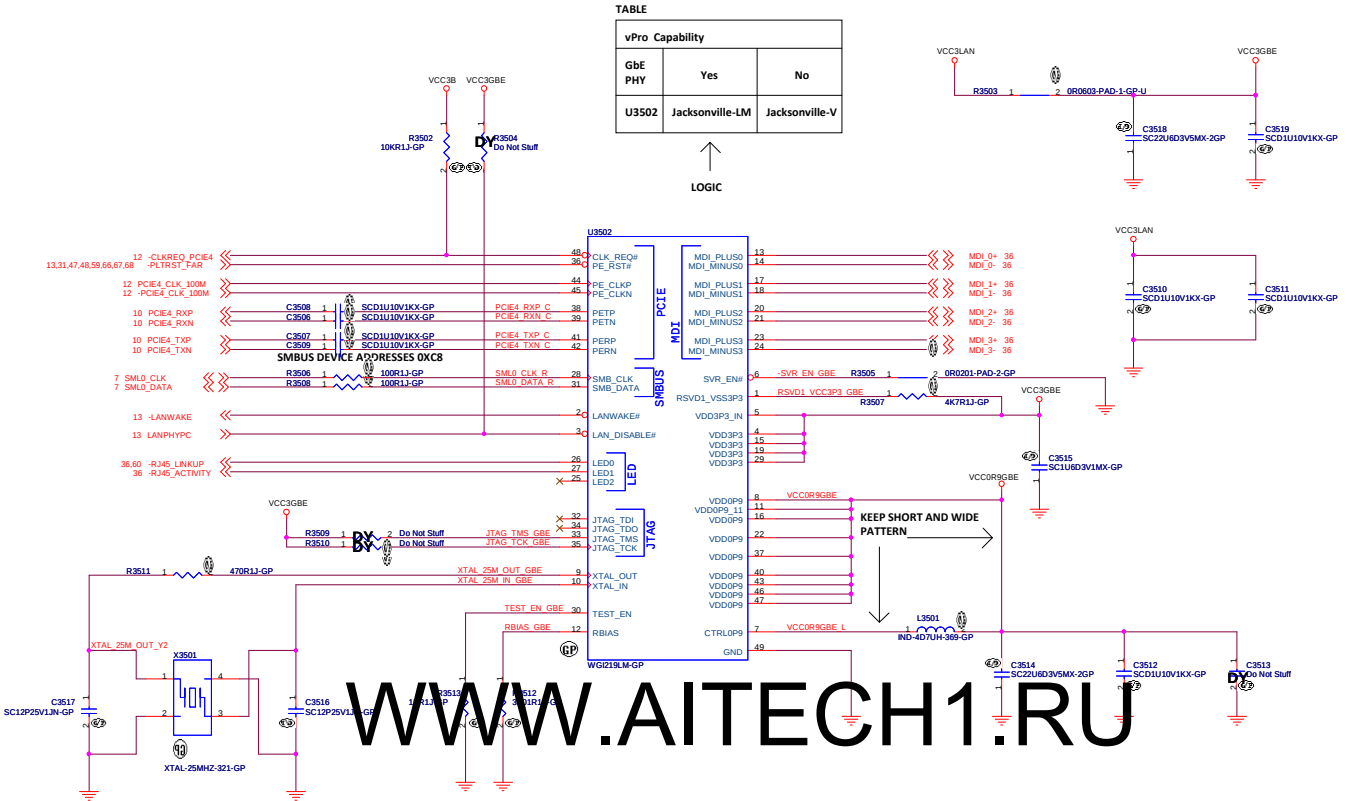
<Core Design>
緯創資通 Wistron Corporation
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: USB POWER/CONN

Size	Document Number	Rev
Custom	TS1	1

Date: Thursday, November 03, 2016 Sheet 33 of 103





X3501
TXC 7R25080002
EPSON Q22FA1280055900
KDS 1ZZNAE25000CC0B

	TXC	EPSON	KDS
X3501	082.30005.0791	082.30006.0331	082.30005.0771
R3511	470 ohm	470 ohm	470 ohm
C3516	12P	12P	12P
C3517	12P	12P	12P

<Core Design>

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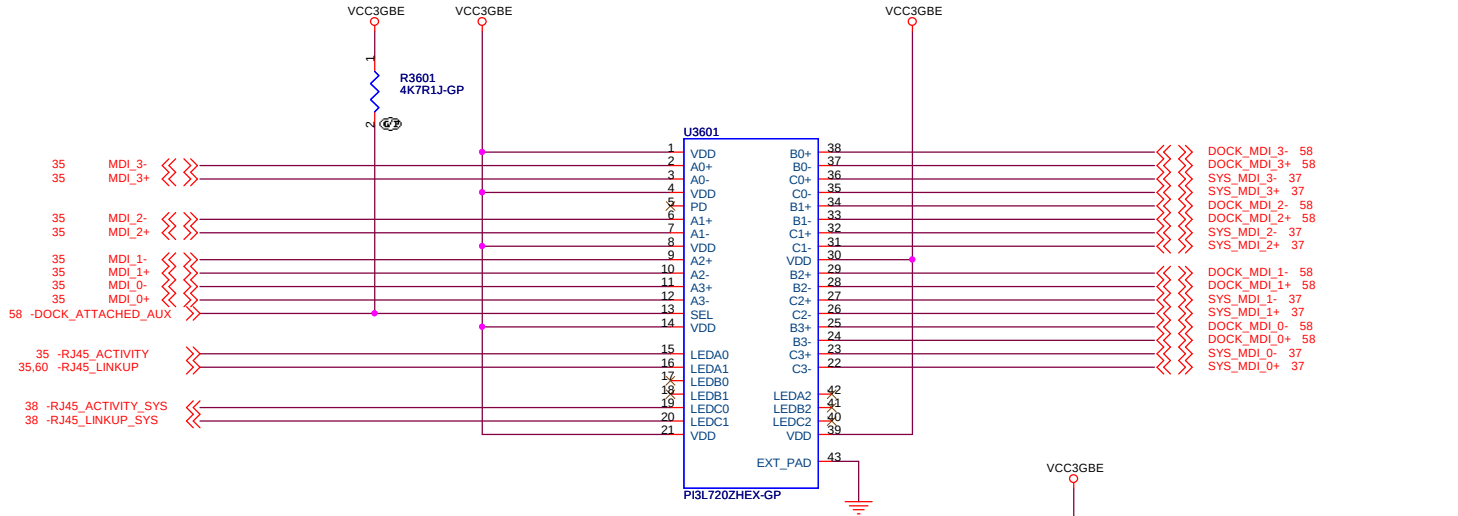
Taipei Hsien 221, Taiwan, R.O.C.

Title: GBE JACKSONVILLE

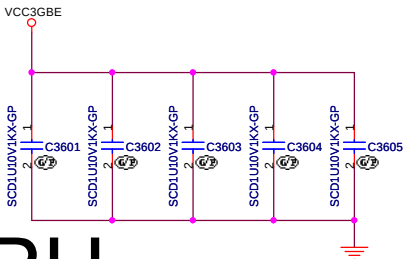
Size	Document Number	Rev
A3	TS1	1

Date: Thursday, November 03, 2016 Sheet 35 of 103



U3601

Vendor	P/N
Pericom	PI3L720ZHE
TI	TS3L501ERUAR



<Core Design>

緯創資通 **Wistron Corporation**
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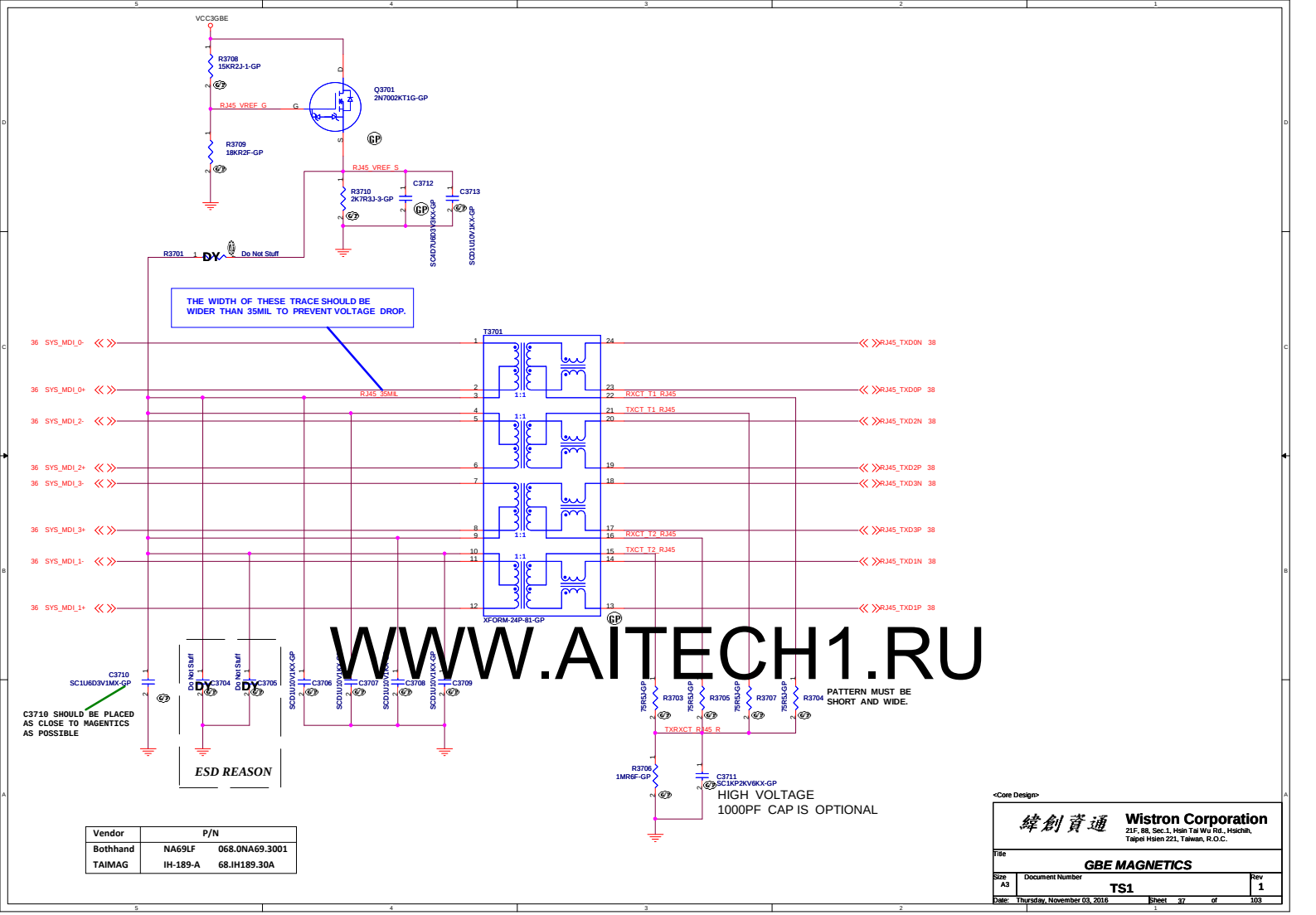
Taipei Hsien 221, Taiwan, R.O.C.

Title: **GBE LAN Switch**

Size	Document Number	Rev
A4	TS1	1

Date: Thursday, November 03, 2016 Sheet 36 of 103



Vendor	P/N	
Bothhand	NA69LF	068.0NA69.3001
TAIMAG	IH-189-A	68.IH189.30A

<Core Design>

緯創資通 Wistron Corporation
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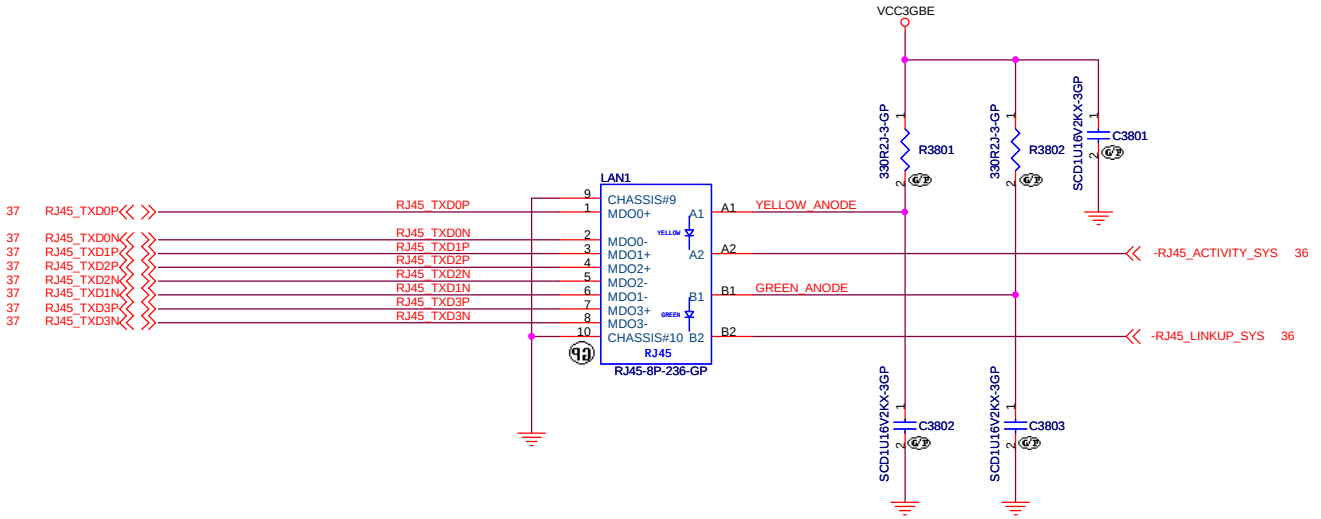
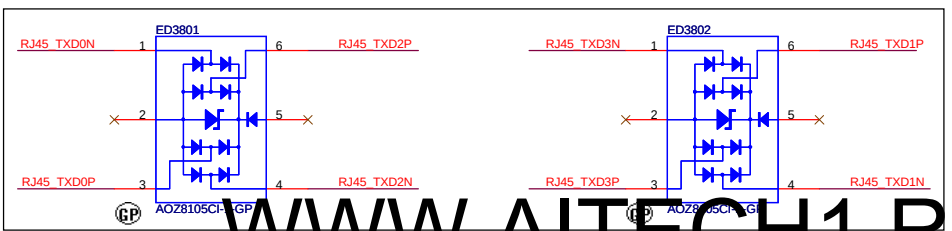
Taipei Hsien 221, Taiwan, R.O.C.

Title: GBE MAGNETICS

Size	Document Number	Rev
A3	TS1	1

Date: Thursday, November 03, 2016 Sheet 37 of 103





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緯創資通 **Wistron Corporation**
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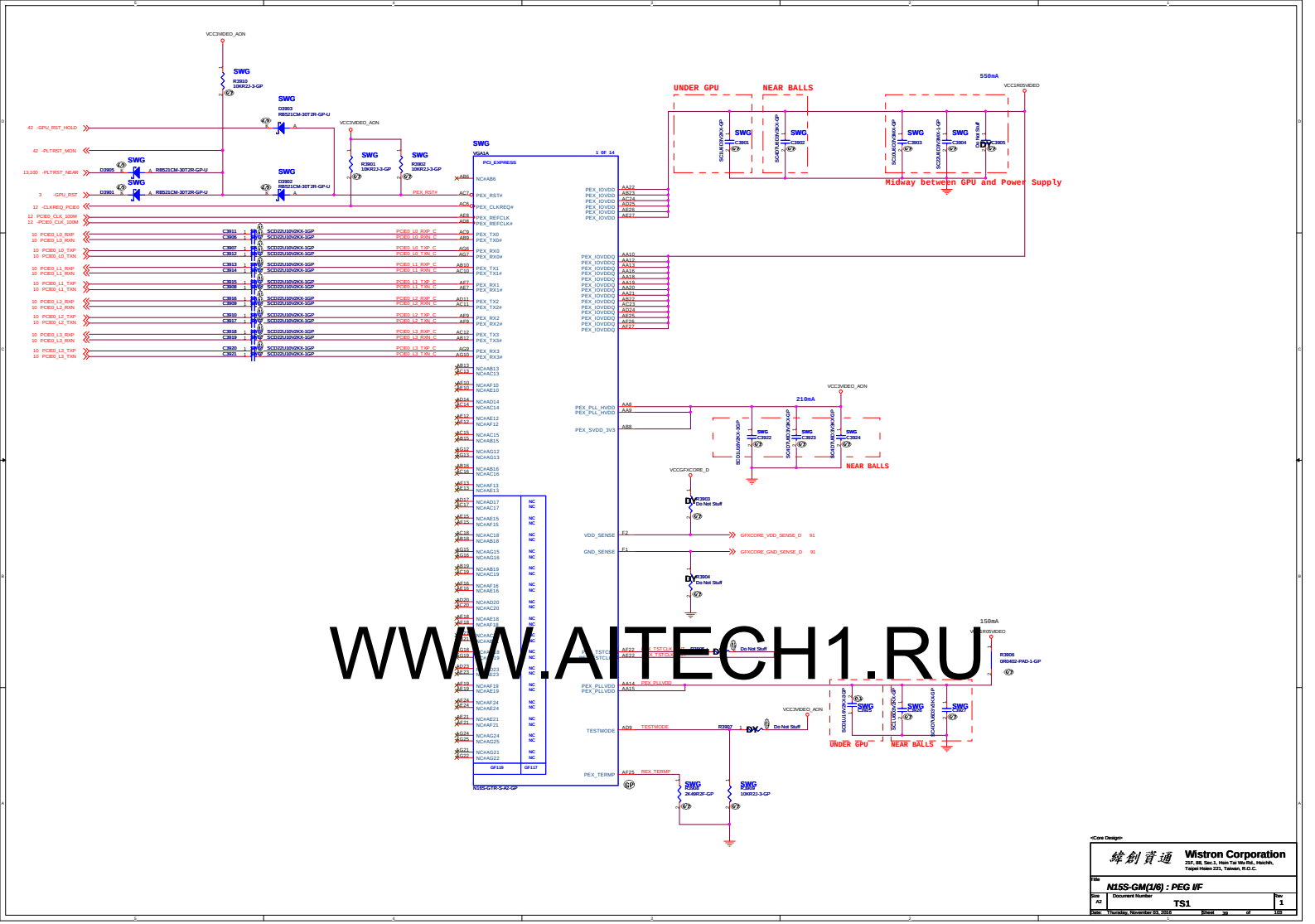
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***RJ45 CONNECTOR***

Size	Document Number	Rev
Custom	TS1	1

Date: Thursday, November 03, 2016 Sheet 38 of 103

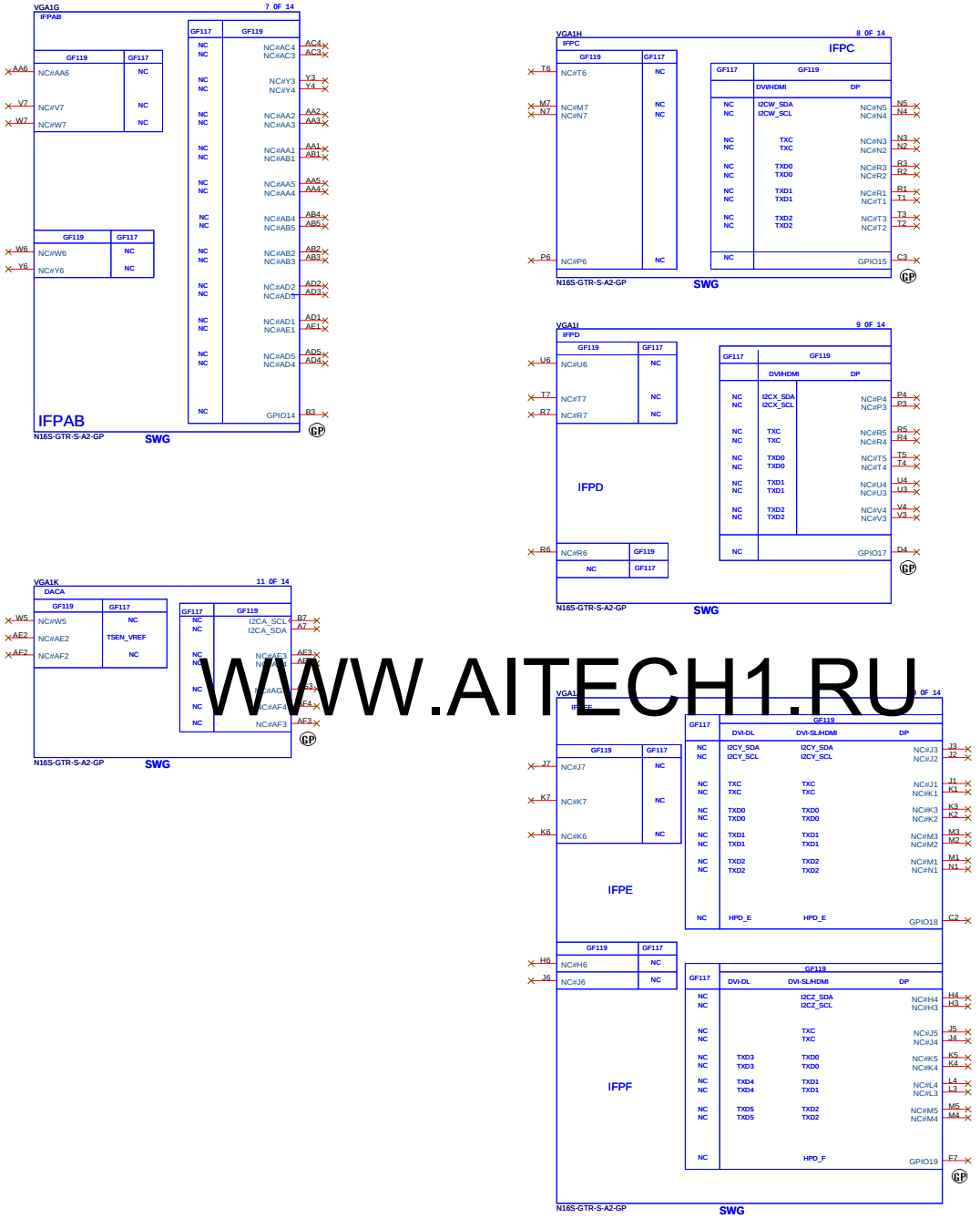


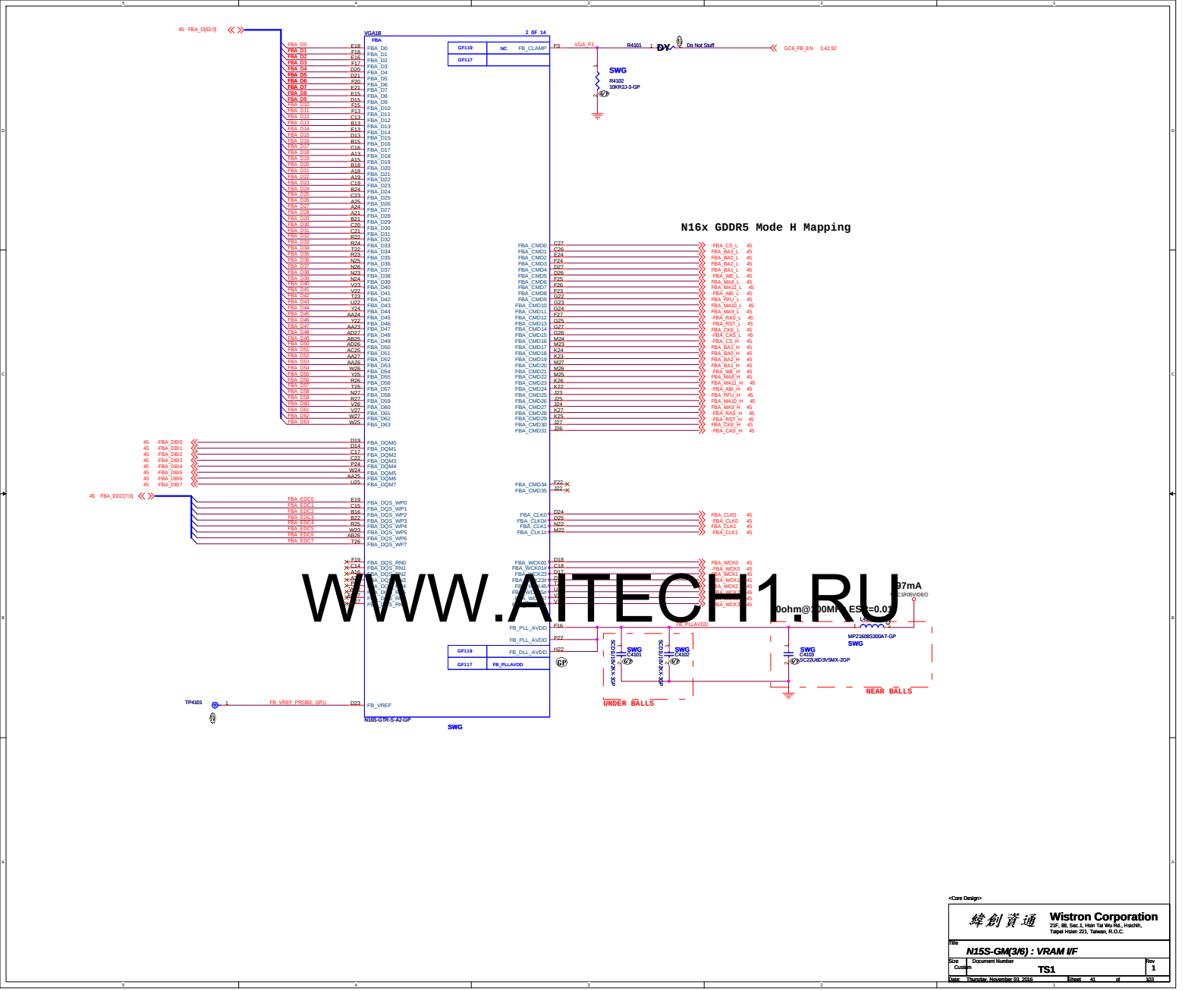
<Core Design>
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: N15S-GM(1/6) : PEG I/F

Size	Document Number	Rev
A2	TS1	1

Date: Thursday, November 03, 2016 Sheet 39 of 100





<Core Design>

緯創資通 Wistron Corporation
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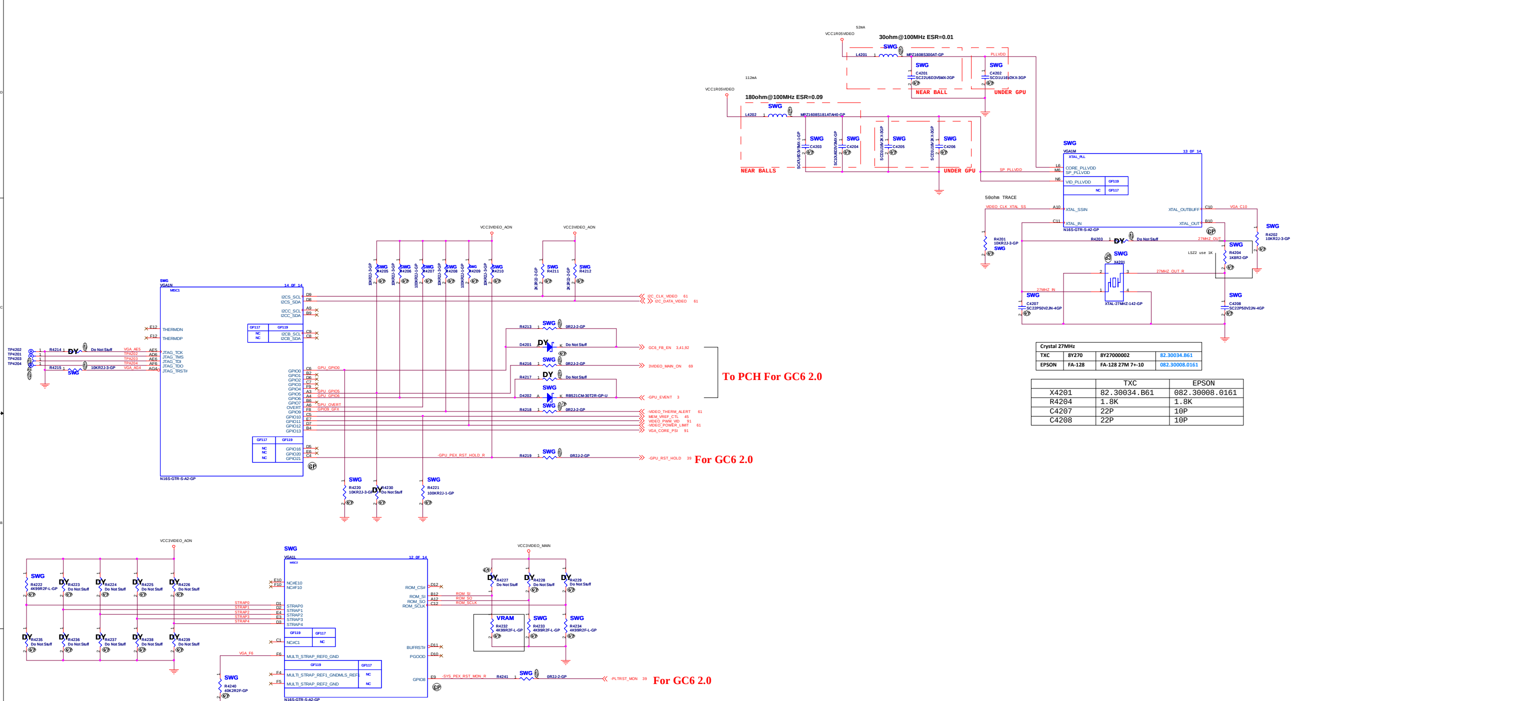
Taipei Hsien 221, Taiwan, R.O.C.

Title: N15S-GM(3/6) : VRAM I/F

Size	Document Number	Rev
Custom	TS1	1

Date: Thursday, November 03, 2016 Sheet 41 of 103



Crystal 27MHz			
TXC	8Y270	8Y27000002	82.30034.B61
EPSON	FA-128	FA-128 27M 7+-10	082.30008.0161

	TXC	EPSON
X4201	82.30034.B61	082.30008.0161
R4204	1.8K	1.8K
C4207	22P	10P
C4208	22P	10P

TABLE
VIDEO MEMORY

[illegible]OM[illegible]SIPD	[illegible]AMSU[illegible]G [illegible]Gb 2[illegible]6Mx3[illegible] S[illegible]RAP[illegible]0000	[illegible]CRON [illegible]Gb 25[illegible]Mx32 ST[illegible]AP:[illegible]001
R422[illegible] PU	N[illegible]_A[illegible]M	NO_[illegible]SM
R4232 PD	4.99Kohm	10Kohm

LOGIC

<Core Design>

緯創資通 **Wistron Corporation**
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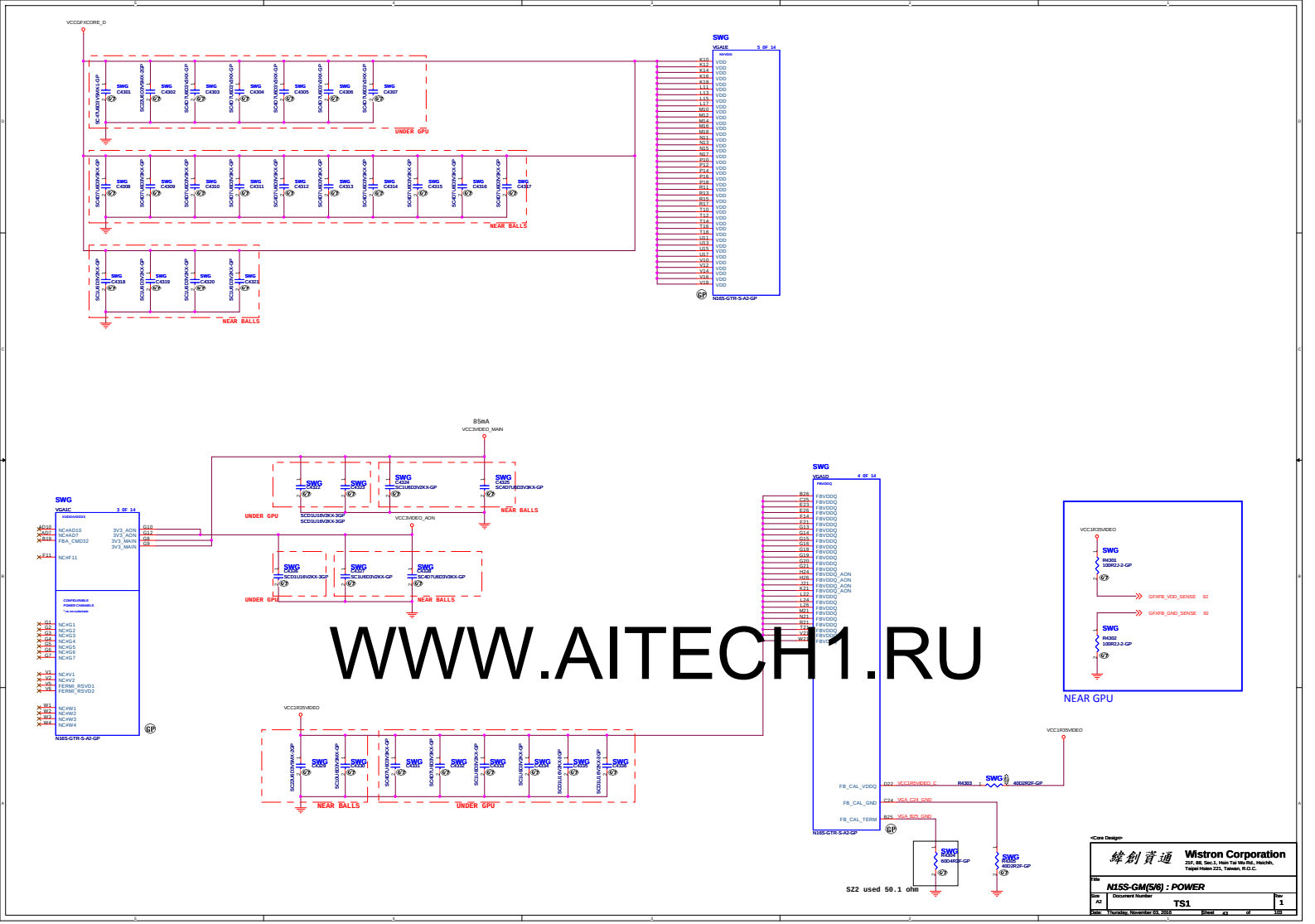
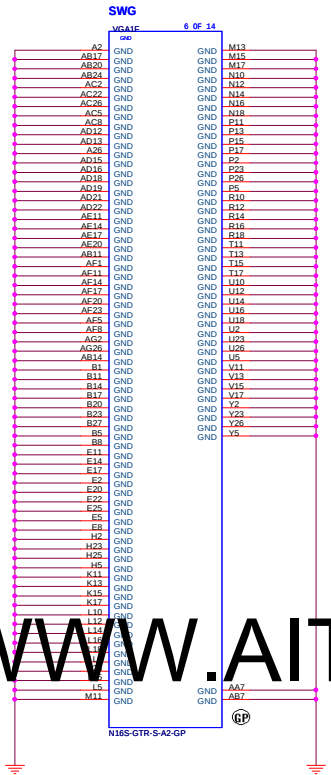
Title: **N15S-GM(4/6) : GPIO**

Size: Custom | Document Number: TS1 | Rev: 1





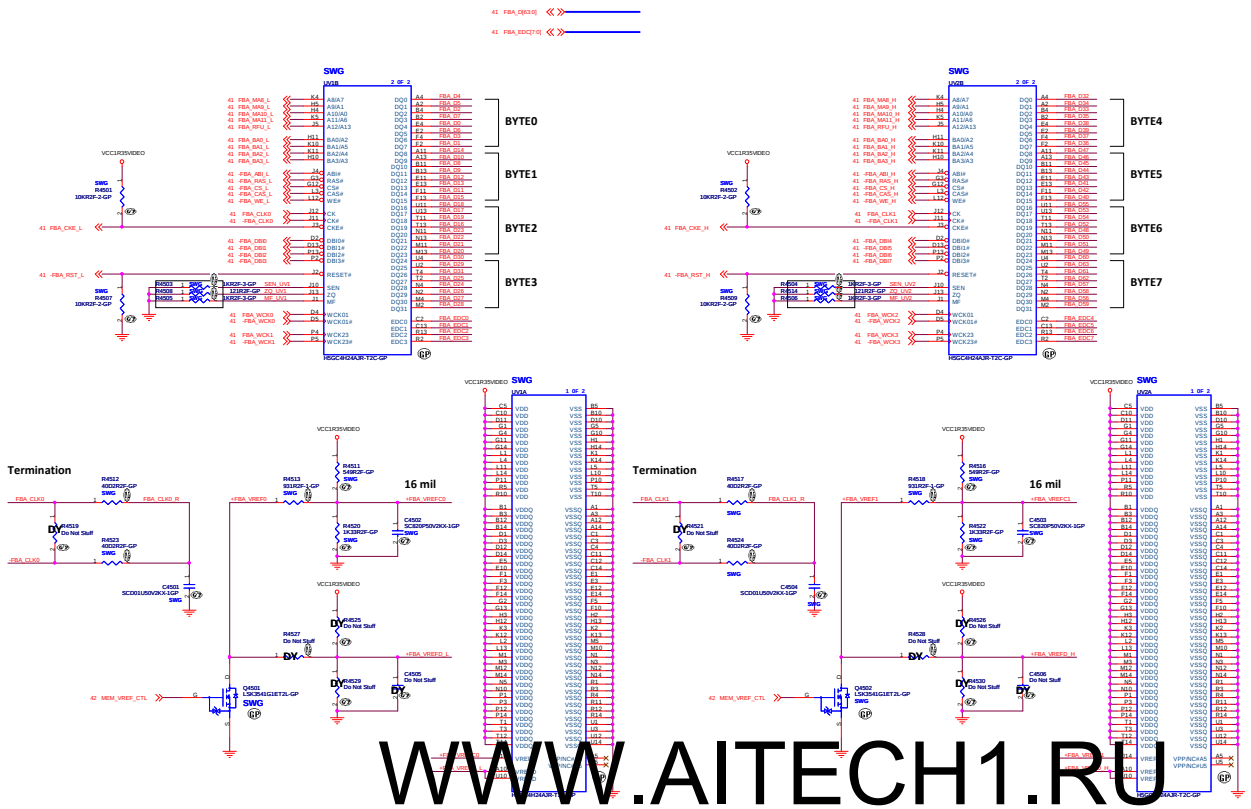
<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *N15S-GM(6/6) : GND*

Size	Document Number	Rev
A3	TS1	1

Date: Thursday, November 03, 2016 Sheet 44 of 103



TS-1	For N16S-GTR (Geforce) For N15M-Q3 (Quadro)	
VRAM	SAMSUNG, GDDR5, 256M x 32, 8Gb	MICRON, GDDR5, 256M x 32, 8Gb
UV1 UV2	K4G80325FB-HC03 (B-die)	MT51J256M32HF-60:A (A-die)
BOM Structure	VS@	VM@

<Core Design>
緯創資通 Wistron Corporation
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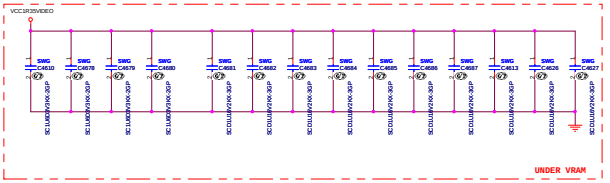
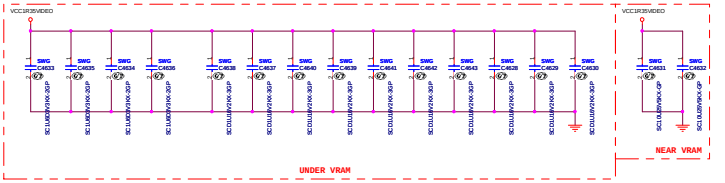
Taipei Hsien 221, Taiwan, R.O.C.
Title: VRAM
Size: A2 | Document Number: TS1 | Rev: 1
Date: Thursday, November 03, 2016 | Sheet 45 of 100

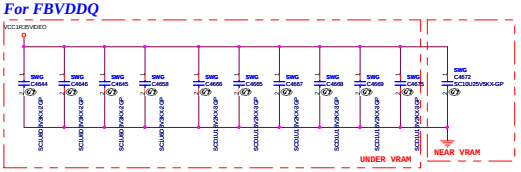
For UV1



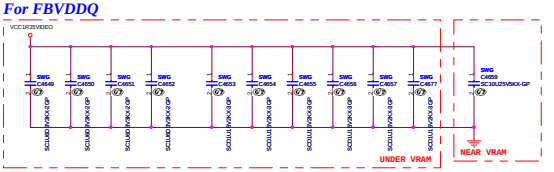
For UV2



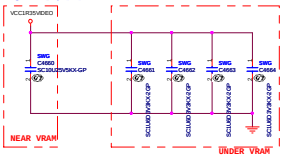
For FBVDDQ



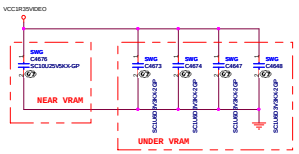
For FBVDDQ



For FBVDD

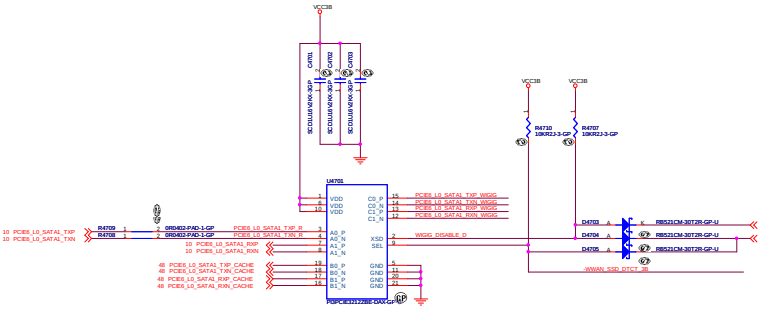


For FBVDD

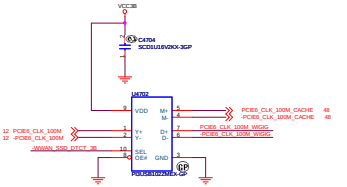


Capacitor Type		Footprint		Population[1] FBVDDQ	Population[1] FBVDD	Location[2]
FBVDD/Q Combined						
0.1 µF	X7R	0402	10	10		Under DRAM
1.0 µF	X7R	0603	4	4		Under DRAM
10 µF	X5R	0805	2	2		Close to DRAM
FBVDD/Q Separate						
0.1 µF	X7R	0402	6	6	0	Under DRAM
1.0 µF	X7R	0603	8	4	4	Under DRAM
10 µF	X5R	0805	2	1	1	Close to DRAM

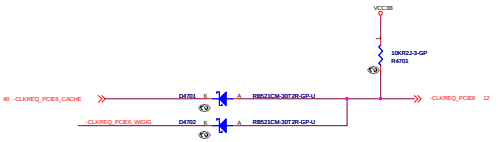
Note:
1. Per sub-partition, for example, per two pieces of ×16 DRAM or one piece of ×32 DRAM.
2. Location is close to DRAM for all decoupling with ×16 DRAM.



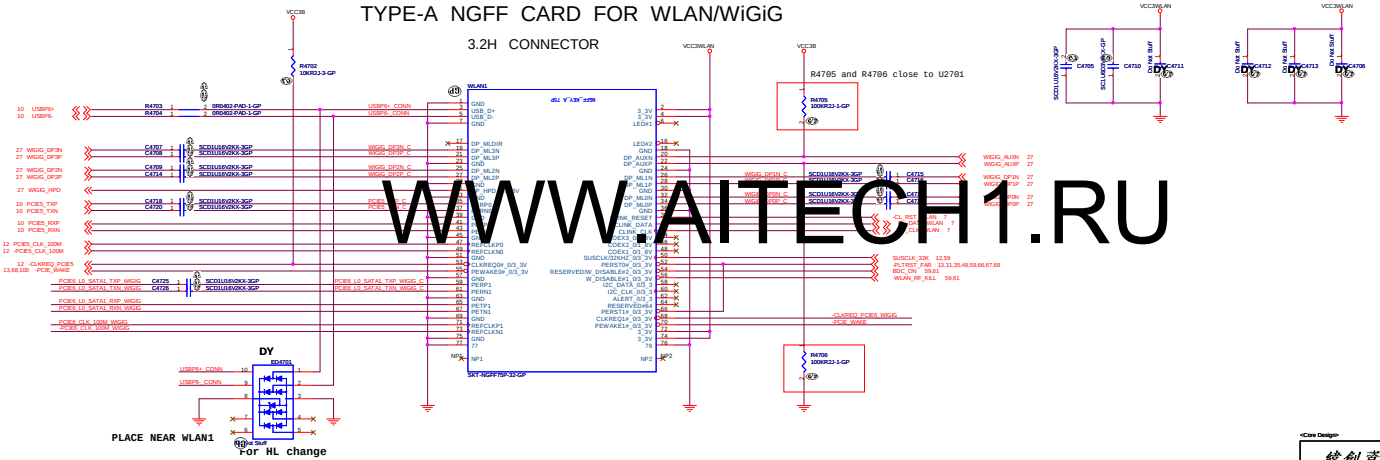
Pericom PI3PCIE3212ZBE 071.33212.0003
NXP CBTL02043ABQ 071.02043.0003
TOSHIBA TC7PCI3212MT 071.73212.0003



Pericom PI3USB102ZME 73.3US10.D03
NXP NX3DV42GU 73.00342.003



	WWAN Slot							
	Optance		SATA Cache		WWAN Card		None	
WiGig_DISABLE	L	H	L	H	L	H	L	H
-WWAN_SSD_DTCT	L	L	L	L	H	H	H	H
SEL(U4701)	L	L	L	L	H	H	H	H
XSD(U4701)	L	L	L	L	L	H	L	H
PCIE6_L0_SATA1	To M.2 Socket2	To M.2 Socket2	To M.2 Socket2	To M.2 Socket2	To M.2 Socket2	Disconnect	To M.2 Socket2	Disconnect
-WWAN_SATA_DTCT	High	High	Low	Low	High	High	High	High
PCIE6_L0_SATA1	PCIe	PCIe	SATA	SATA	PCIe	PCIe	PCIe	PCIe



<Core Design>

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M.2 SOCKET 1 MODULE I/F

Size: A2 | Document Number: TS1 | Rev: 1

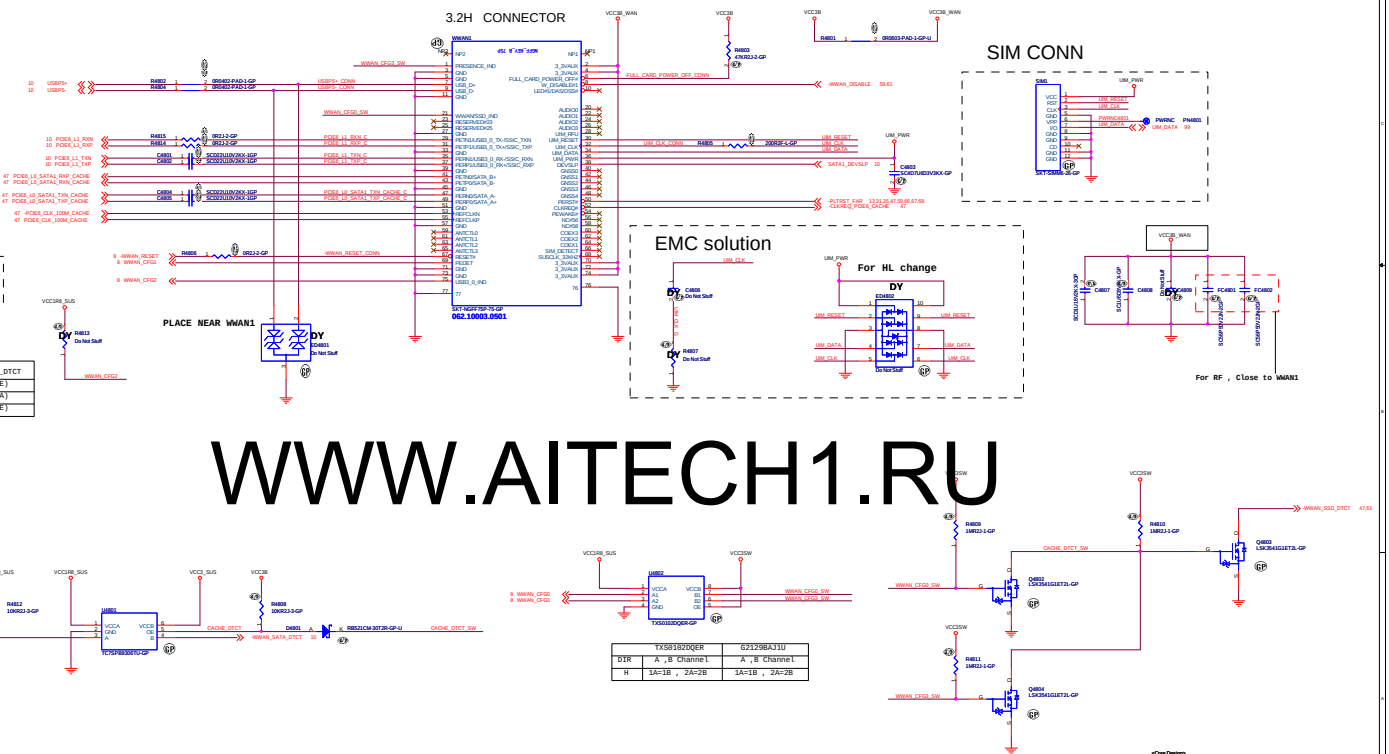
Date: Thursday, November 03, 2005 | Sheet 47 of 100

TABLE:

State #	Module Configuration Decodes				Module Type and Main Host Interface	Port Configuration
	CONFIG_0 (Pin 21)	CONFIG_3 (Pin 1)	CONFIG_2 (Pin 75)	CONFIG_1 (Pin 69)		
0	GND	GND	GND	GND	SSD - SATA	N/A
1	GND	GND	GND	NC	SSD - PCIe	N/A
2	GND	GND	NC	GND	WWAN - PCIe	0
3	GND	GND	NC	NC	WWAN - PCIe	1
4	GND	NC	GND	GND	WWAN - USB 3.0	0
5	GND	NC	GND	NC	WWAN - USB 3.0	1
6	GND	NC	NC	GND	WWAN - USB 3.0	2
7	GND	NC	NC	NC	WWAN - USB 3.0	3
8	NC	GND	GND	GND	WWAN - SSIC	0
9	NC	GND	GND	NC	WWAN - SSIC	1
10	NC	GND	NC	GND	WWAN - SSIC	2
11	NC	GND	NC	NC	WWAN - SSIC	3
12	NC	NC	GND	GND	WWAN - PCIe	2
13	NC	NC	GND	NC	WWAN - PCIe	3
14	NC	NC	NC	GND	RFU	N/A
15	NC	NC	NC	NC	No Module Present	N/A

TYPE-B NGFF CARD FOR WWAN

3.2H CONNECTOR



CACHE_DTCT	WWAN_CFG1	~WWAN_SATA_DTCT
1	1	1 (PCIE)
1	0	0 (SATA)
0	X	1 (PCIE)

CFG0	CFG3	CACHE_DTCT
0	0	1 SSD
0	1	0 WWAN
1	0	
1	1	NA

TXS0102DQER		G2129BAJ1U
DIR	A ,B Channel	A ,B Channel
H	1A=1B , 2A=2B	1A=1B , 2A=2B

•Core Design
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File: M.2 SOCKET 2 MODULE I/F

Size: Custom | Document Number: TS1 | Rev: 1

Date: Thursday, November 03, 2011 | Sheet 48 of 103

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WWW.AITECH1.RU

<Core Design>

緯創資通

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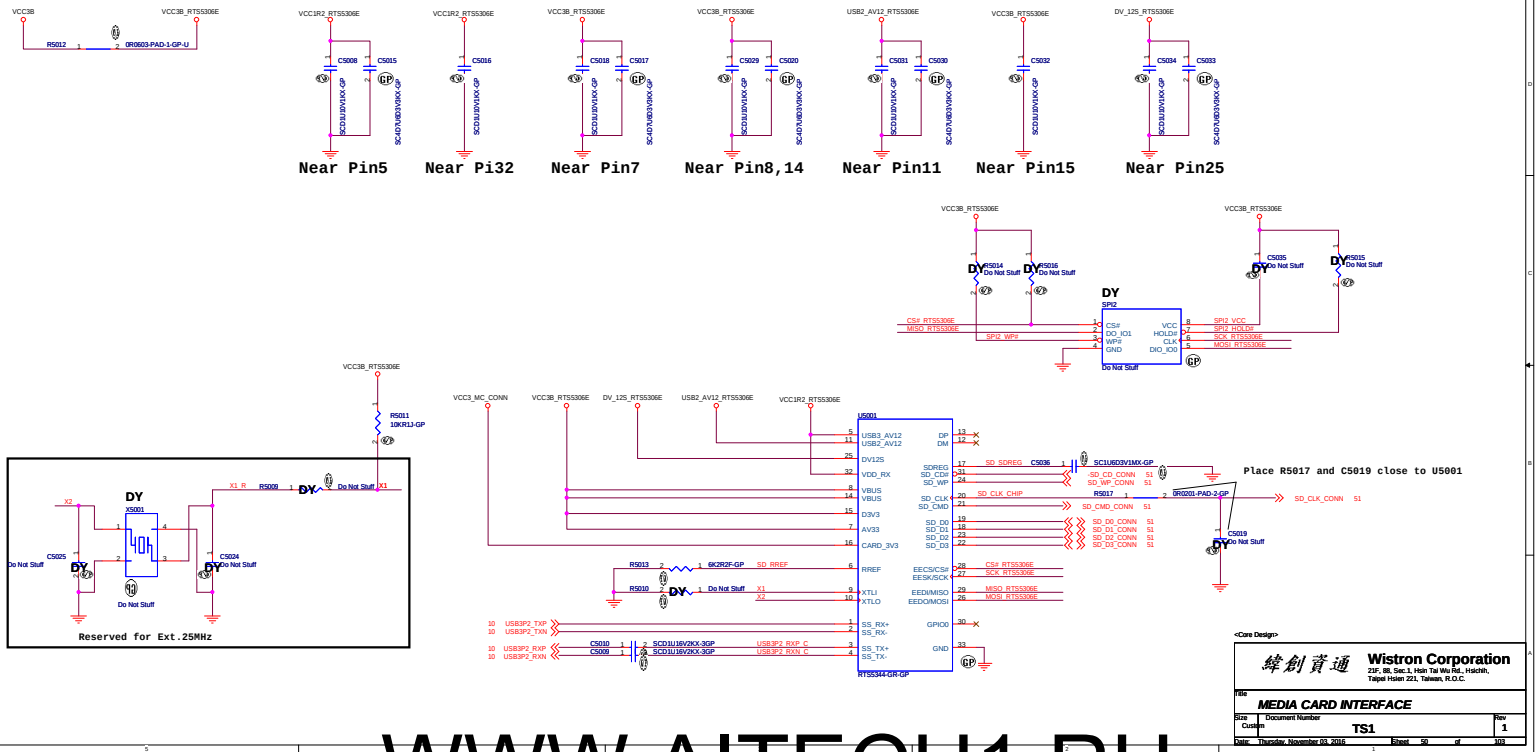
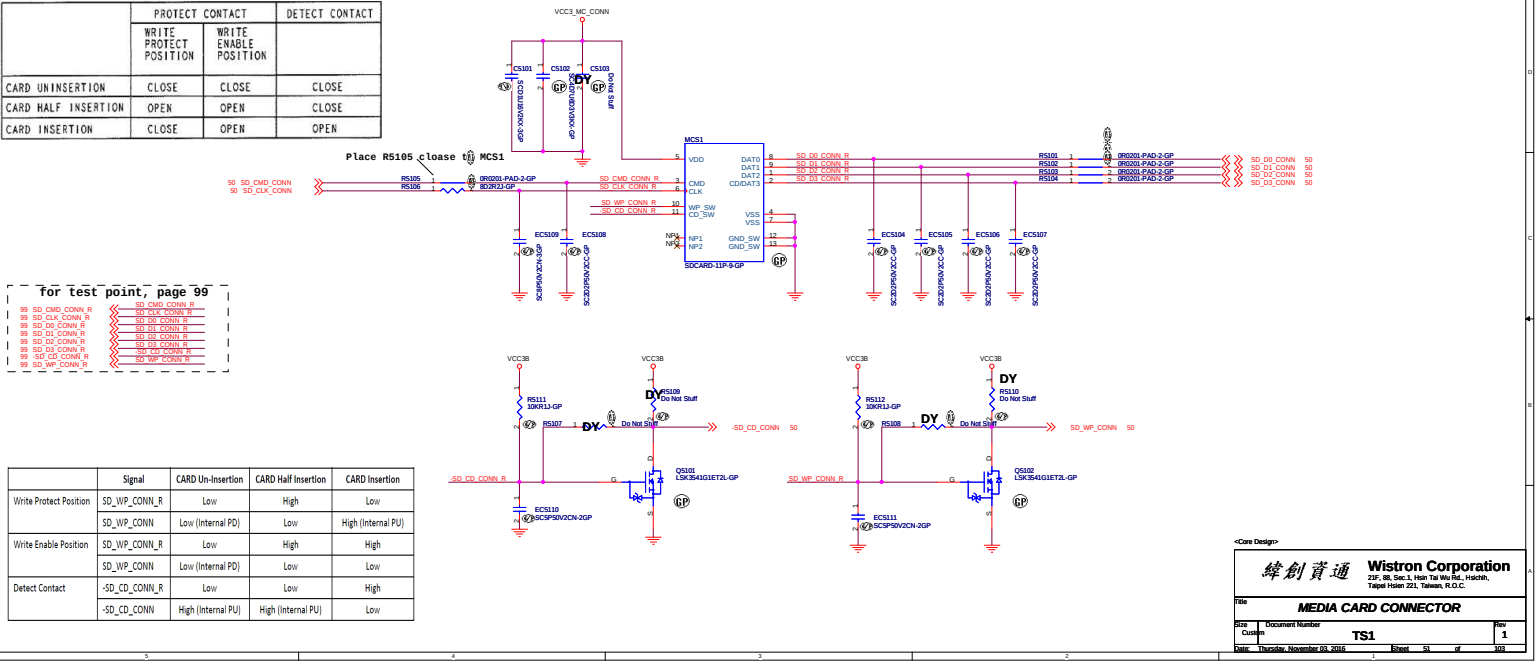
Title	***BLANK***	
Size: A	Document Number: **TS1**	Rev: **1**
Date: Thursday, November 03, 2016	Sheet 49 of 103	



	PROTECT CONTACT		DETECT CONTACT
	WRITE PROTECT POSITION	WRITE ENABLE POSITION	
CARD UNINSERTION	CLOSE	CLOSE	CLOSE
CARD HALF INSERTION	OPEN	OPEN	CLOSE
CARD INSERTION	CLOSE	OPEN	OPEN



	Signal	CARD Un-Insertion	CARD Half Insertion	CARD Insertion
Write Protect Position	SD_WP_CONN_R	Low	High	Low
	SD_WP_CONN	Low (Internal PD)	Low	High (Internal PU)
Write Enable Position	SD_WP_CONN_R	Low	High	High
	SD_WP_CONN	Low (Internal PD)	Low	Low
Detect Contact	-SD_CD_CONN_R	Low	Low	High
	-SD_CD_CONN	High (Internal PU)	High (Internal PU)	Low

<Core Design>

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: MEDIA CARD CONNECTOR

Size	Document Number	Rev
Custom	TS1	1

Date: Thursday, November 03, 2016 Sheet 51 of 103

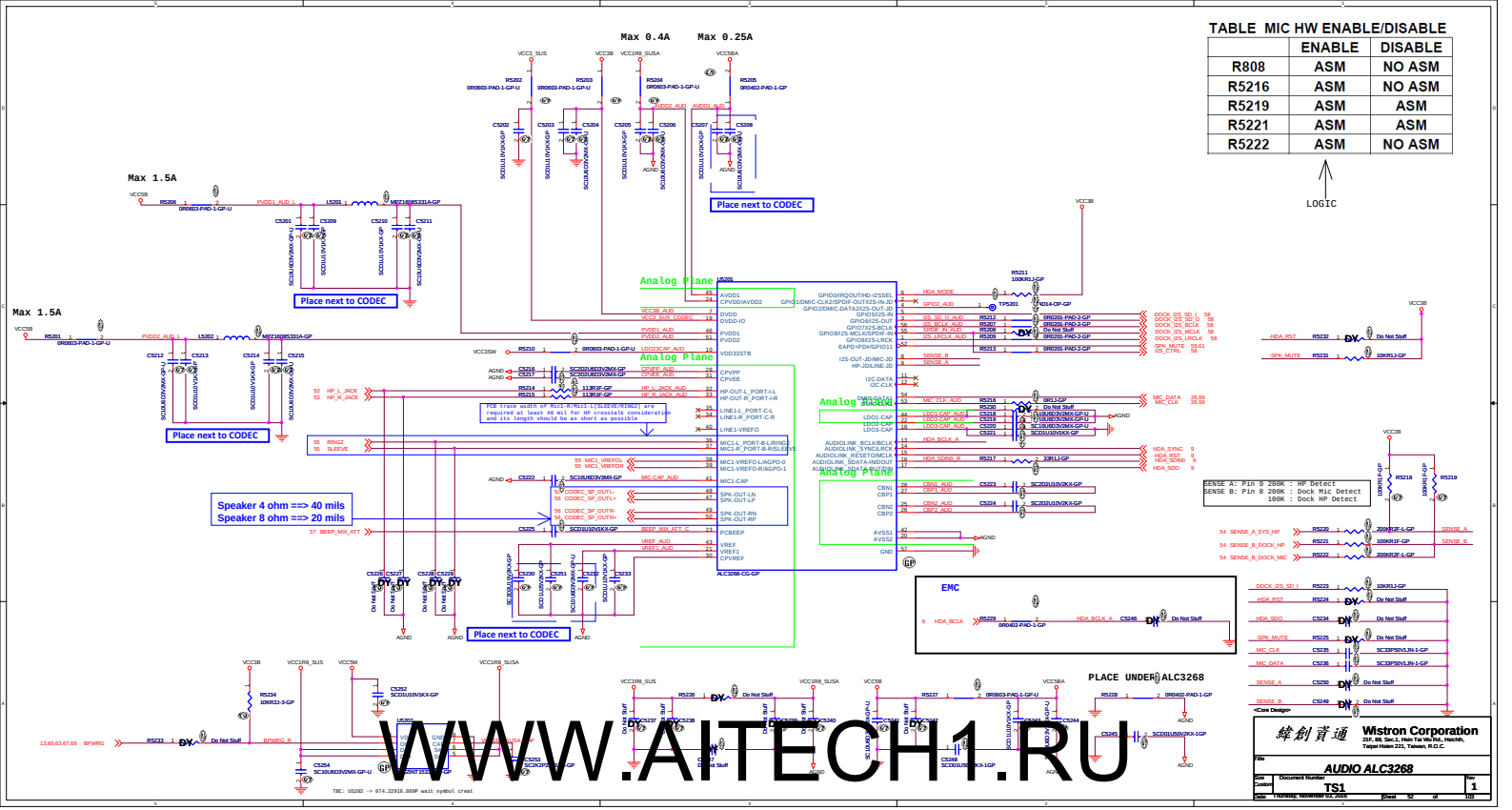
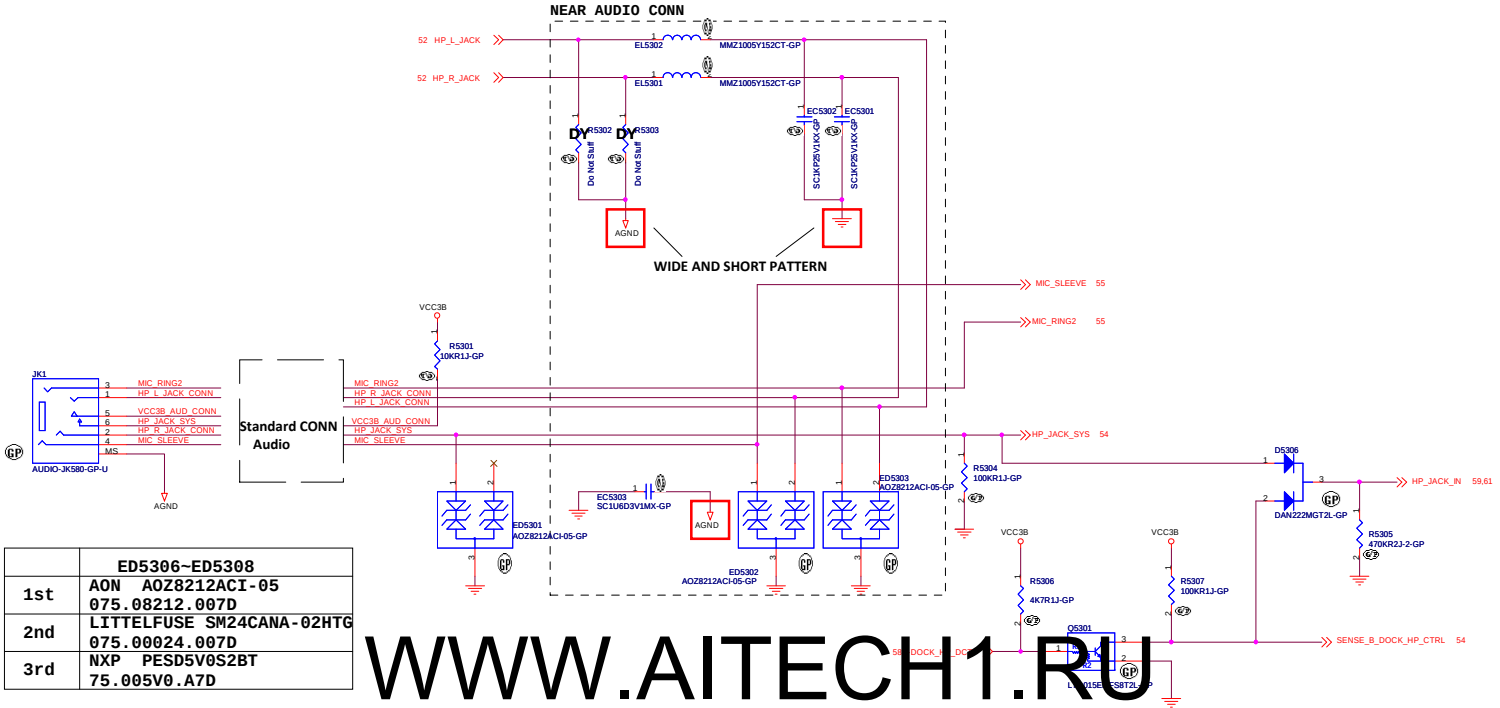


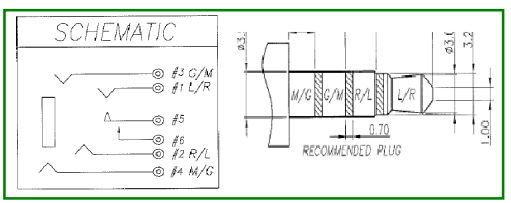
TABLE MIC HW ENABLE/DISABLE

	ENABLE	DISABLE
R808	ASM	NO ASM
R5216	ASM	NO ASM
R5219	ASM	ASM
R5221	ASM	ASM
R5222	ASM	NO ASM



	ED5306~ED5308
1st	AON AOZ8212ACI-05 075.08212.007D
2nd	LITTELFUSE SM24CANA-02HTG 075.00024.007D
3rd	NXP PESD5V0S2BT 75.005V0.A7D

Audio Jack



<Core Design>

緯創資通 Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: AUDIO CONNECTOR

Size: A3 | Document Number: TS1 | Rev: 1

Date: Thursday, November 03, 2016 | Sheet 53 of 103

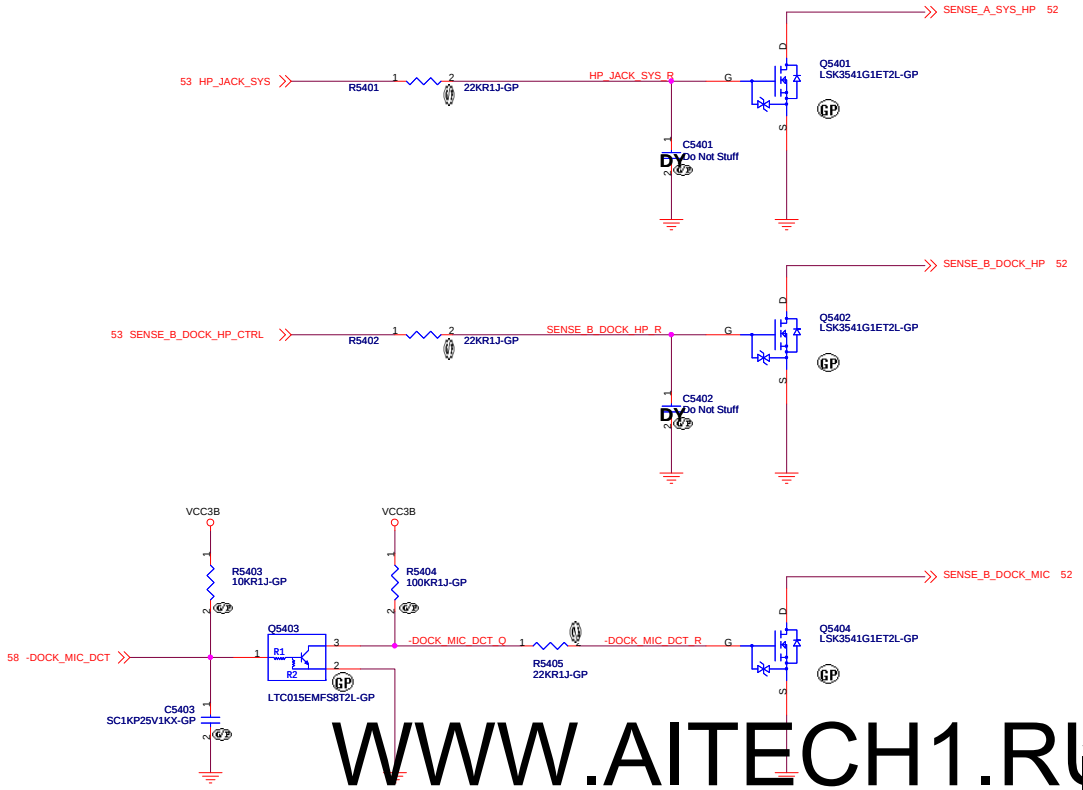


TABLE MIC HW ENABLE/DISABLE

	ENABLE	DISABLE
R5403	ASM	NO ASM
R5404	ASM	NO ASM
R5405	ASM	NO ASM
Q5403	ASM	NO ASM
Q5404	ASM	NO ASM

LOGIC

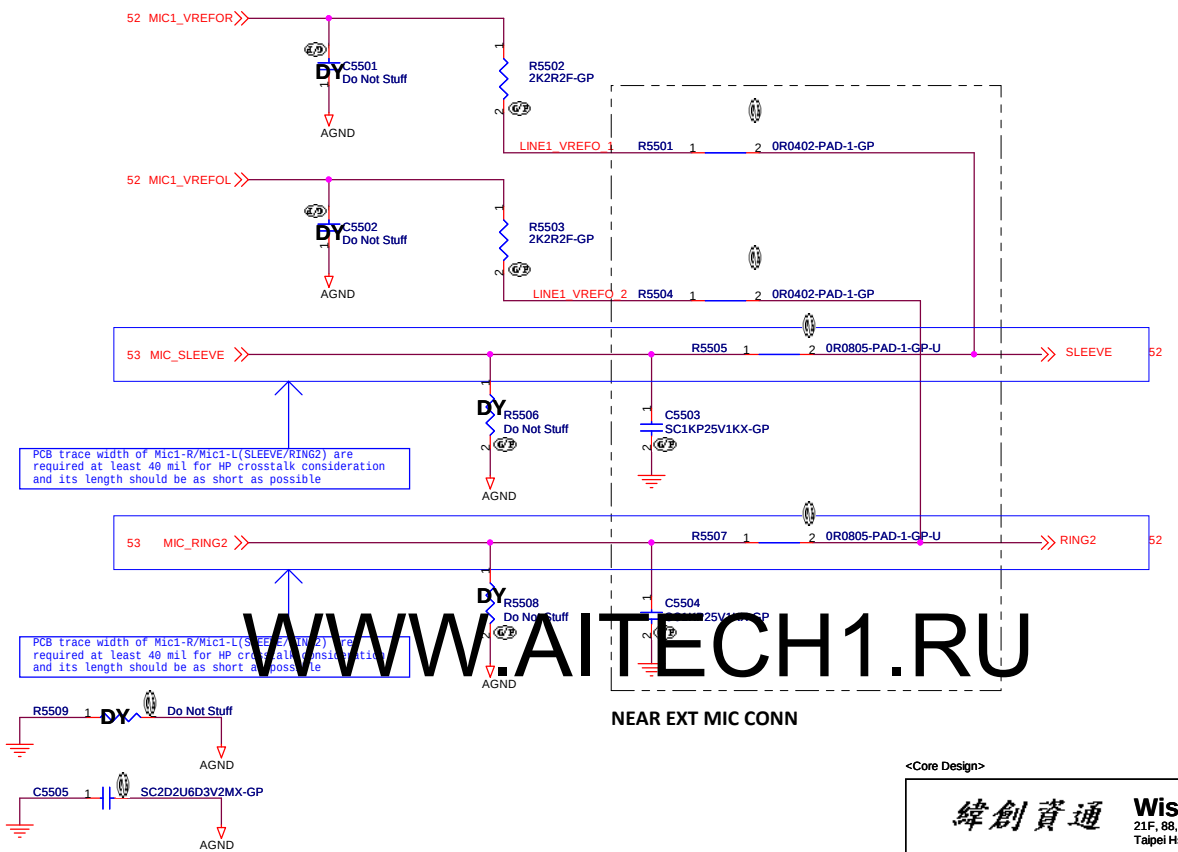
<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: AUDIO JACK SENSE

Size: Custom | Document Number: TS1 | Rev: 1

Date: Thursday, November 03, 2016 | Sheet 54 of 103



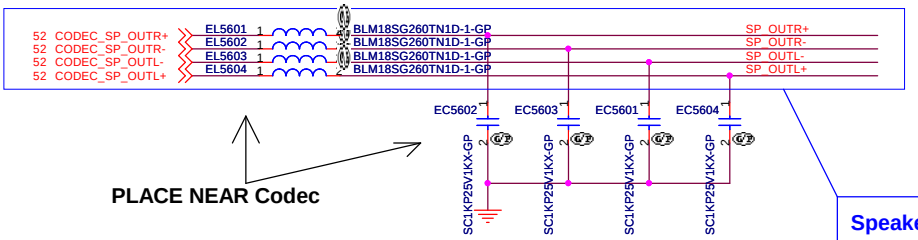
<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***AUDIO EXT MIC I/F***

Size	Document Number	Rev
A4	TS1	1

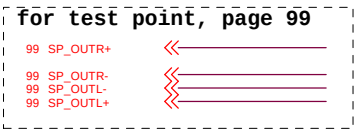
Date: Thursday, November 03, 2016 Sheet 55 of 103

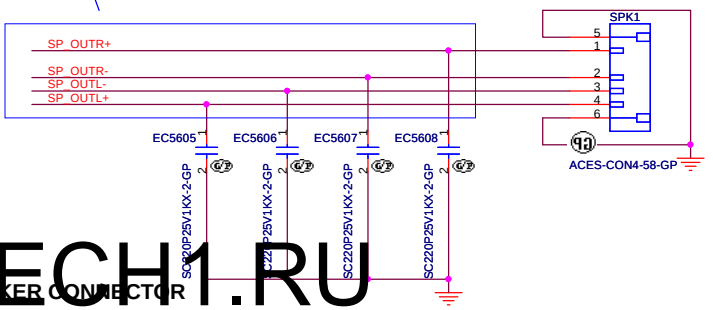


PLACE NEAR Codec

Speaker 4 ohm ==> 40 mils
Speaker 8 ohm ==> 20 mils

ALC3268 speaker output part





PLACE NEAR SPEAKER CONNECTOR

<Core Design>

緯創資通 Wistron Corporation
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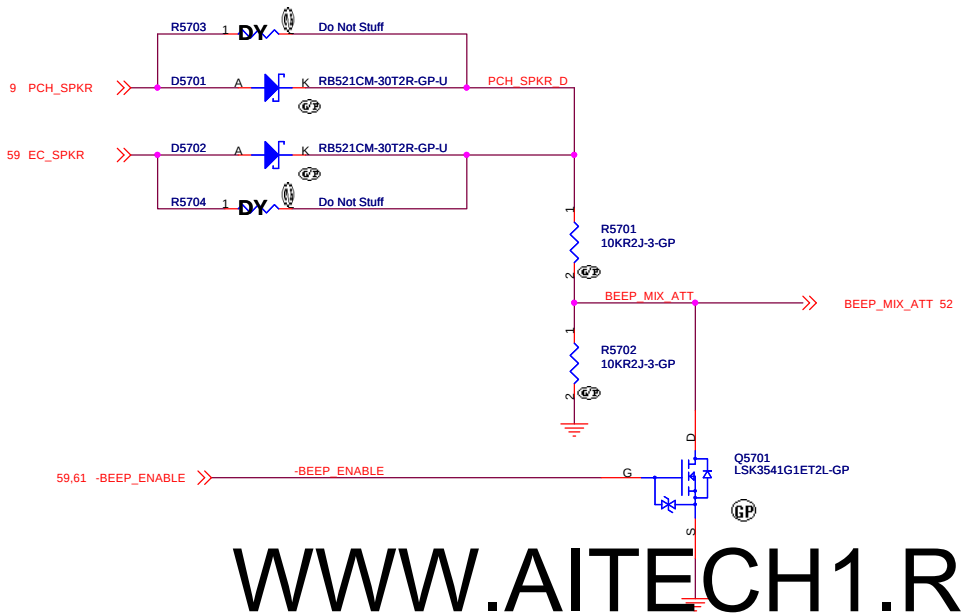
Taipei Hsien 221, Taiwan, R.O.C.

Title: AUDIO SPEAKER

Size	Document Number	Rev
A4	TS1	1

Date: Thursday, November 03, 2016 Sheet 56 of 103



<Core Design>

緯創資通 **Wistron Corporation**
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Taipei Hsien 221, Taiwan, R.O.C.

Title: **AUDIO BEEP**

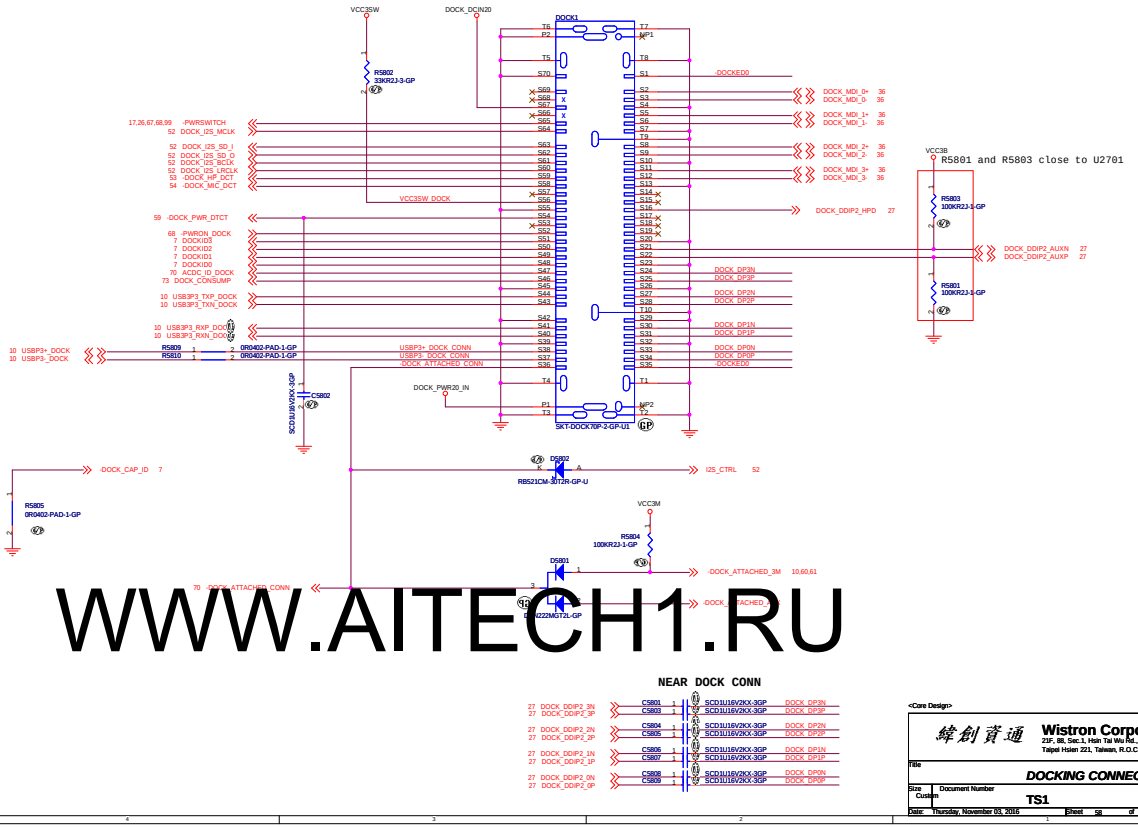
Size	Document Number	Rev
A4	TS1	1

Date: Thursday, November 03, 2016 Sheet 57 of 103

LOGIC

TABLE

ID	DOCKING SUPPORT	NON-SUPPORT
DOCK1	ASM	NO ASM
R5802	ASM	NO ASM
D5801	ASM	NO ASM
D5802	ASM	NO ASM
R5804	ASM	NO ASM
C5802	ASM	ASM
R5809	ASM	NO ASM
R5810	ASM	NO ASM
C5801	ASM	NO ASM
C5803	ASM	NO ASM
C5804	ASM	NO ASM
C5805	ASM	NO ASM
C5806	ASM	NO ASM
C5807	ASM	NO ASM
C5808	ASM	NO ASM
C5809	ASM	NO ASM
R5803	ASM	NO ASM
R5801	ASM	NO ASM
R5805	ASM	NO ASM



NEAR DOCK CONN

<Core Design>

Wistron Corporation
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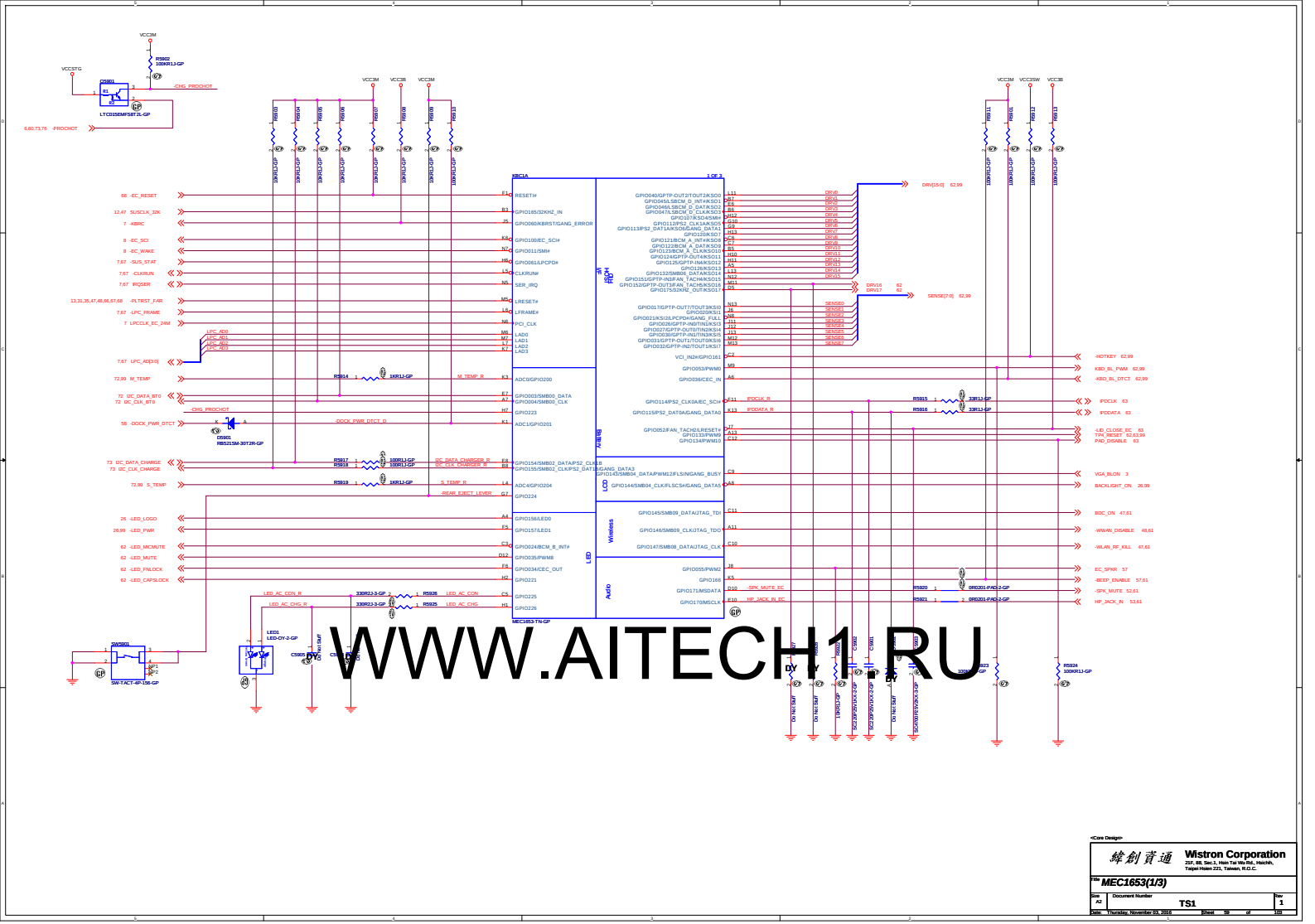
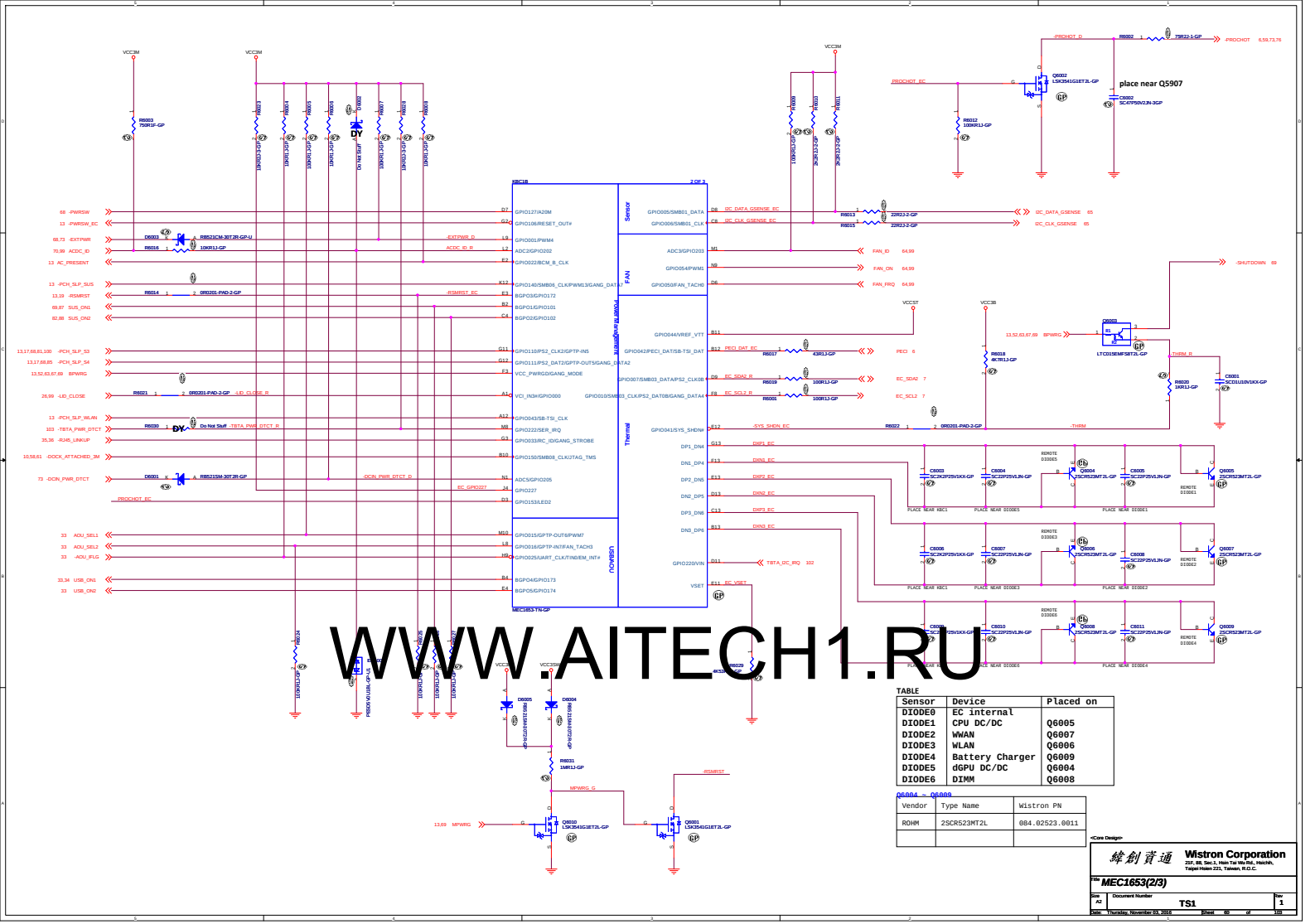
Taipei Hsien 221, Taiwan, R.O.C.

Title: DOCKING CONNECTOR

Size: Custom | Document Number: TS1 | Rev: 1

Date: Thursday, November 03, 2016 | Sheet 58 of 103





TABLE

Sensor	Device	Placed on
DIODE0	EC internal	
DIODE1	CPU DC/DC	Q6005
DIODE2	WWAN	Q6007
DIODE3	WLAN	Q6006
DIODE4	Battery Charger	Q6009
DIODE5	dGPU DC/DC	Q6004
DIODE6	DIMM	Q6008

Q6004 ~ Q6009

Vendor	Type Name	Wistron PN
ROHM	2SCR523MT2L	084.02523.0011

<Core Design>

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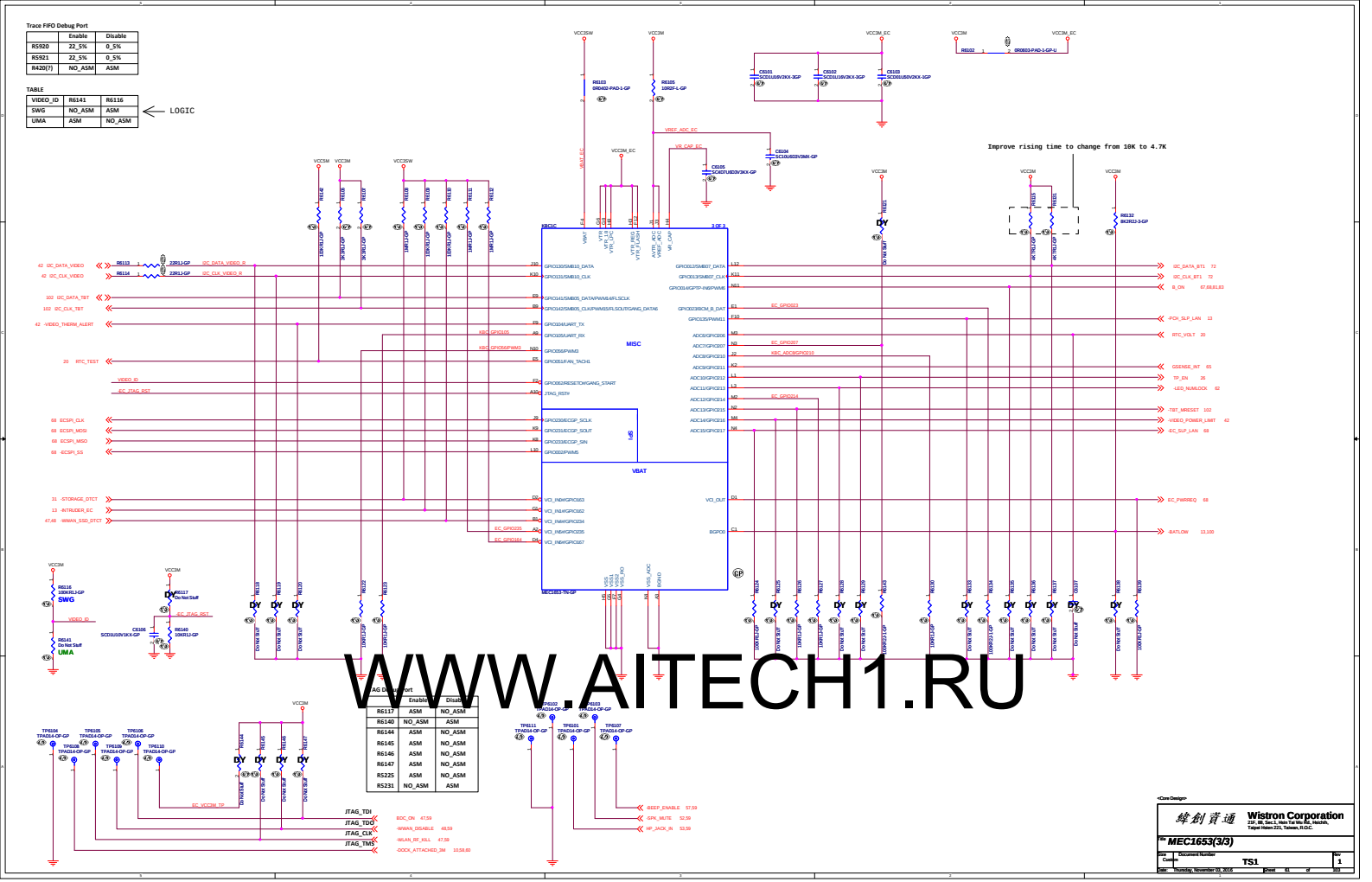
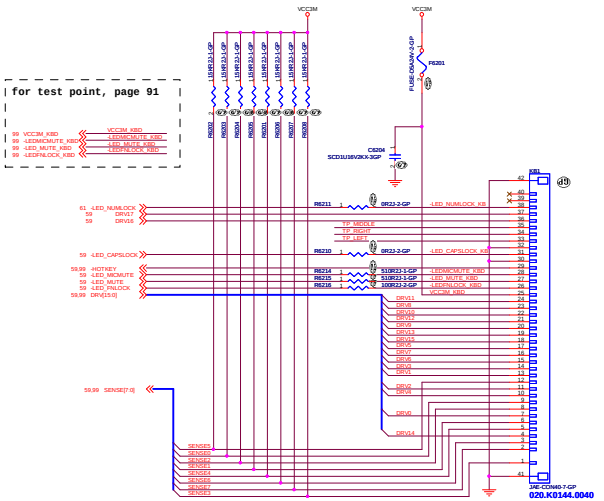
Taipei Hsien 221, Taiwan, R.O.C.

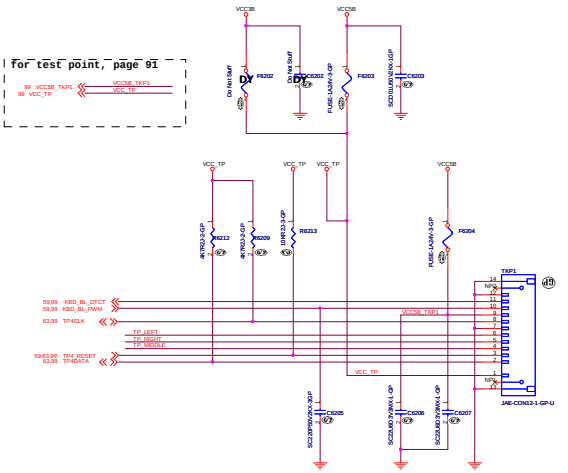
Title: MEC1653(2/3)

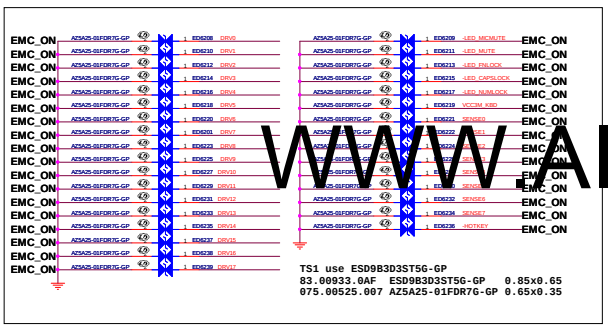
Size: A2 | Document Number: TS1 | Rev: 1

Date: Thursday, November 03, 2016 | Sheet 60 of 100





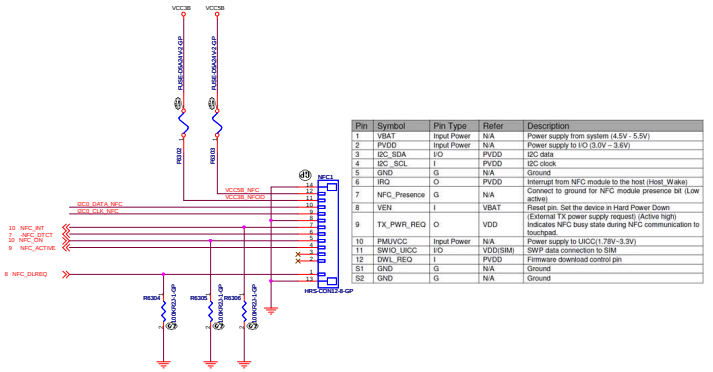




<Core Design>

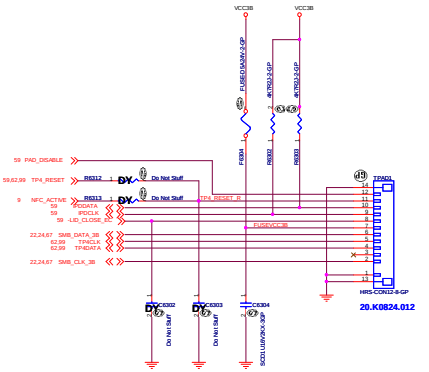
緯創資通	Wistron Corporation	
	21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	KEYBOARD/TRACK POINT	
Size: A2	Document Number: TS1	Rev: 1
Date: Thursday, November 03, 2016	Sheet 62 of 100	

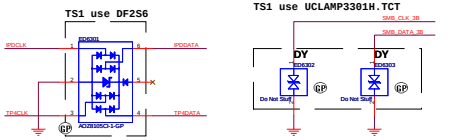
NFC



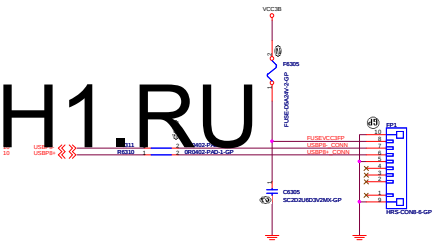
Pin	Symbol	Pin Type	Refer	Description
1	VBAT	Input Power	N/A	Power supply from system (4.5V - 5.5V)
2	PVDD	Input Power	N/A	Power supply to I/O (3.0V – 3.6V)
3	I2C_SDA	I/O	PVDD	I2C data
4	I2C_SCL	I	PVDD	I2C clock
5	GND	G	N/A	Ground
6	IRQ	O	PVDD	Interrupt from NFC module to the host (Host_Wake)
7	NFC_Presence	G	N/A	Connect to ground for NFC module presence bit (Low active)
8	VEN	I	VBAT	Reset pin. Set the device in Hard Power Down
9	TX_PWR_REQ	O	VDD	(External TX power supply request) (Active high) Indicates NFC busy state during NFC communication to touchpad.
10	PMUVCC	Input Power	N/A	Power supply to UICC(1.78V~3.3V)
11	SWIO_UICC	I/O	VDD(SIM)	SWP data connection to SIM
12	DWL_REQ	I	PVDD	Firmware download control pin
S1	GND	G	N/A	Ground
S2	GND	G	N/A	Ground

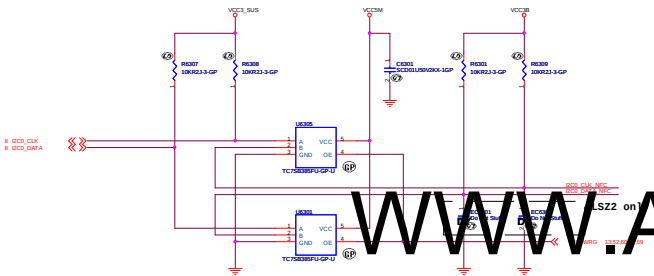
TOUCH PAD



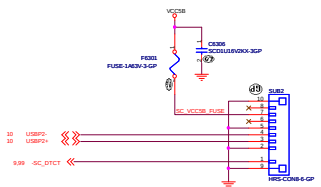


FINGER PRINT READER



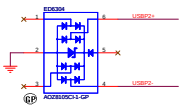


SMART CARD READER



for test point, page 91

99 SC_VCC5B_FUSE → SC_VCC5B_FUSE



<Core Design>
緯創資通 Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: TOUCH PAD/NFC/FPR

Size	Document Number	Rev
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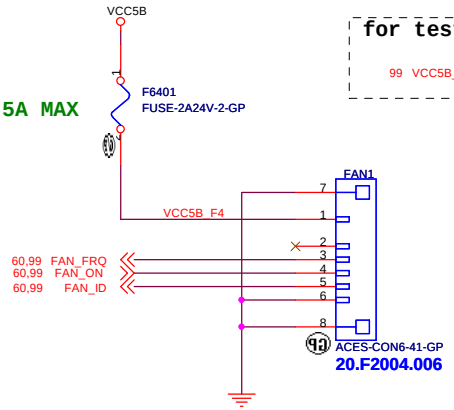
FAN

FAN CURRENT IS 0.5A MAX
FUSE 2.0A



for test point, page 91

99 VCC5B_F4 <<< VCC5B_F4

<Core Design>

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Title	FAN CONNECTOR	
Size A4	Document Number TS1	Rev 1
Date: Thursday, November 03, 2016	Sheet 64 of 103	

TABLE

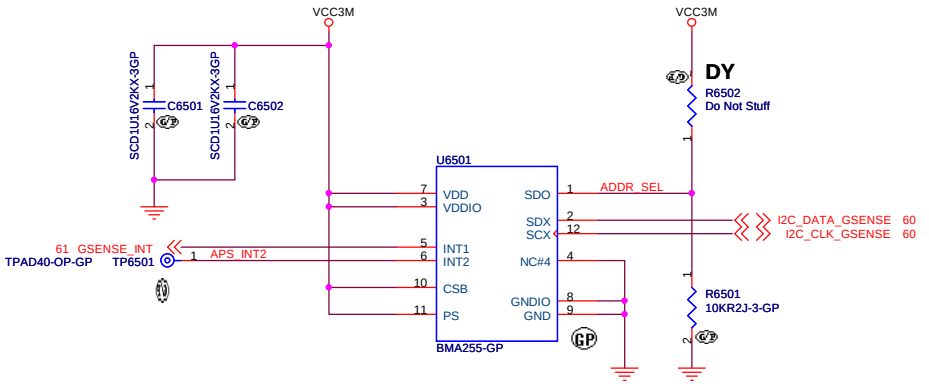
CSB	Mode Selection
H	I2C Mode
L	SPI Mode

Logic

TABLE

P/N	ADDR_SEL	Address
BMA255	H	32h (W) & 33h (R)
	L	30h (W) & 31h (R)
KX022-1020	H	3Eh (W) & 3Fh (R)
	L	3Ch (W) & 3Dh (R)

LOGIC



<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title: ***APS G-SENSOR***

Size	Document Number	Rev
A4	TS1	1

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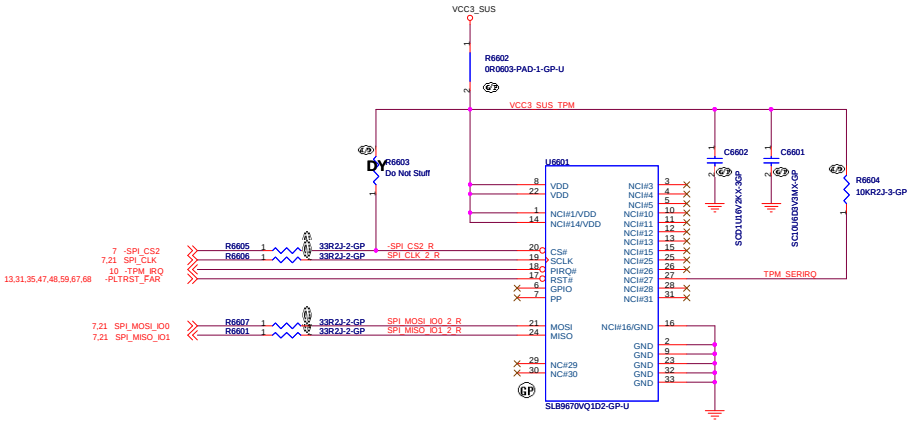

TABLE

Pin No	TCG PTP Spec (v38)	Infineon SLB9670VQ2.0 FW7.60	ST Micro ST33HTPH2E32AHA6	Nuvoton NPCT650LB0YX
1	VDD	VDD	NC	VSB
2	GND	GND	GND	NC
3	GPIO	NC	NC	GPX/GPIO2
4	GPIO	NC	PP	PP
5	NC	NC	NC	TEST
6	VNC/GPIO	GPIO	NC	GPIO3
7	GPIO/VDD	PP	GPIO	NC
8	VDD	VDD	NC	VDD
9	GND	GND	NC	GND
10	VNC	NC	NC	NC
11	NC	NC	NC	NC
12	NC	NC	NC	Reserved
13	VNC/GPIO	NC	NC	GPIO4
14	VDD	NC	NC	VDD
15	NC	NC	NC	DNC
16	GND	NC	NC	GND
17	SPI_RST#	RST#	SPI_RST#	SPI_RST#
18	SPI_PIRQ#	PIRQ#	SPI_IRQ#	SPI_IRQ#
19	SPI_CLK	SCLK	SPI_CLK	SCLK
20	SPI_CS#	CS#	SPI_CS#	SCS#
21	MOSI	MOSI	MOSI	MOSI
22	VDD	VDD	VPS	VDD
23	GND	GND	NC	GND
24	MISO	MISO	MISO	MISO
25	NC	NC	NC	NC
26	NC	NC	NC	NC
27	NC	NC	NC	(SERIRQ)
28	NC	NC	NC	DNC
29	VNC/GPIO	NC	NC	GPIO0
30	VNC/GPIO	NC	NC	GPIO1
31	VNC	NC	NC	NC
32	GND	GND	NC	GND

<Core Design>

緯創資通 Wistron Corporation
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Title: DISCRETE TPM 1.2

Size	Document Number	Rev
A3	TS1	1

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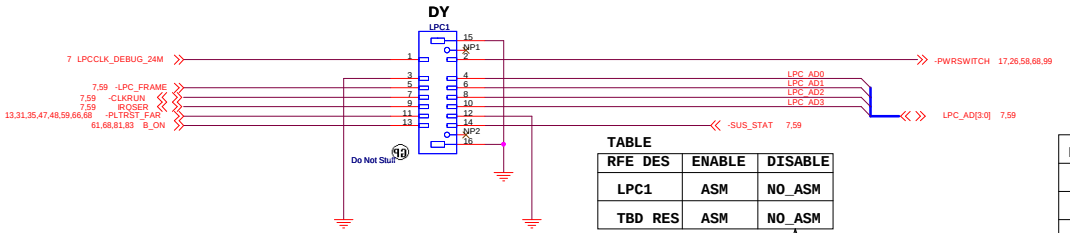
Lenovo Debug Tool I/F



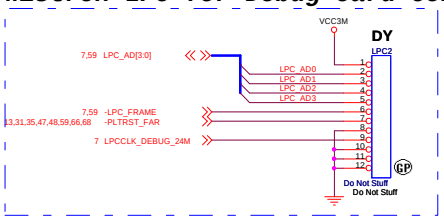
TABLE

RFE DES	ENABLE	DISABLE
LPC1	ASM	NO_ASM
TBD RES	ASM	NO_ASM

LOGIC

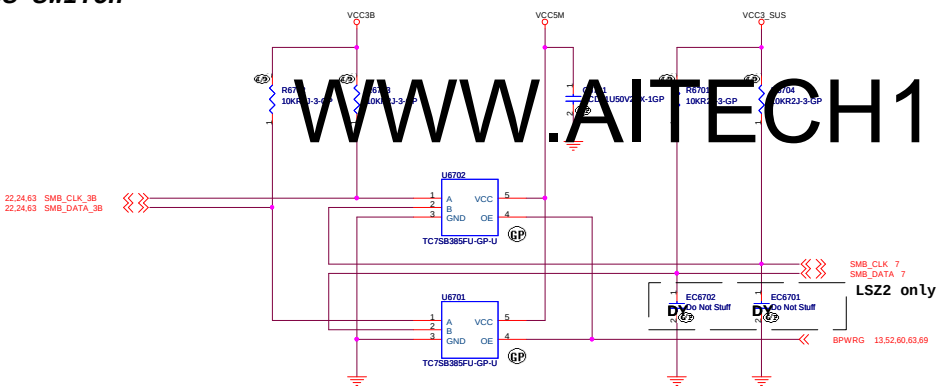
LEVEL	LPC1
SDV	ASM
FVT	No ASM
SIT	TBD
SVT	TBD

Wistron LPC for Debug Card Connector



LEVEL	LPC2
SDV	ASM
FVT	No ASM
SIT	TBD
SVT	TBD

SMBUS SWITCH



<Core Design>

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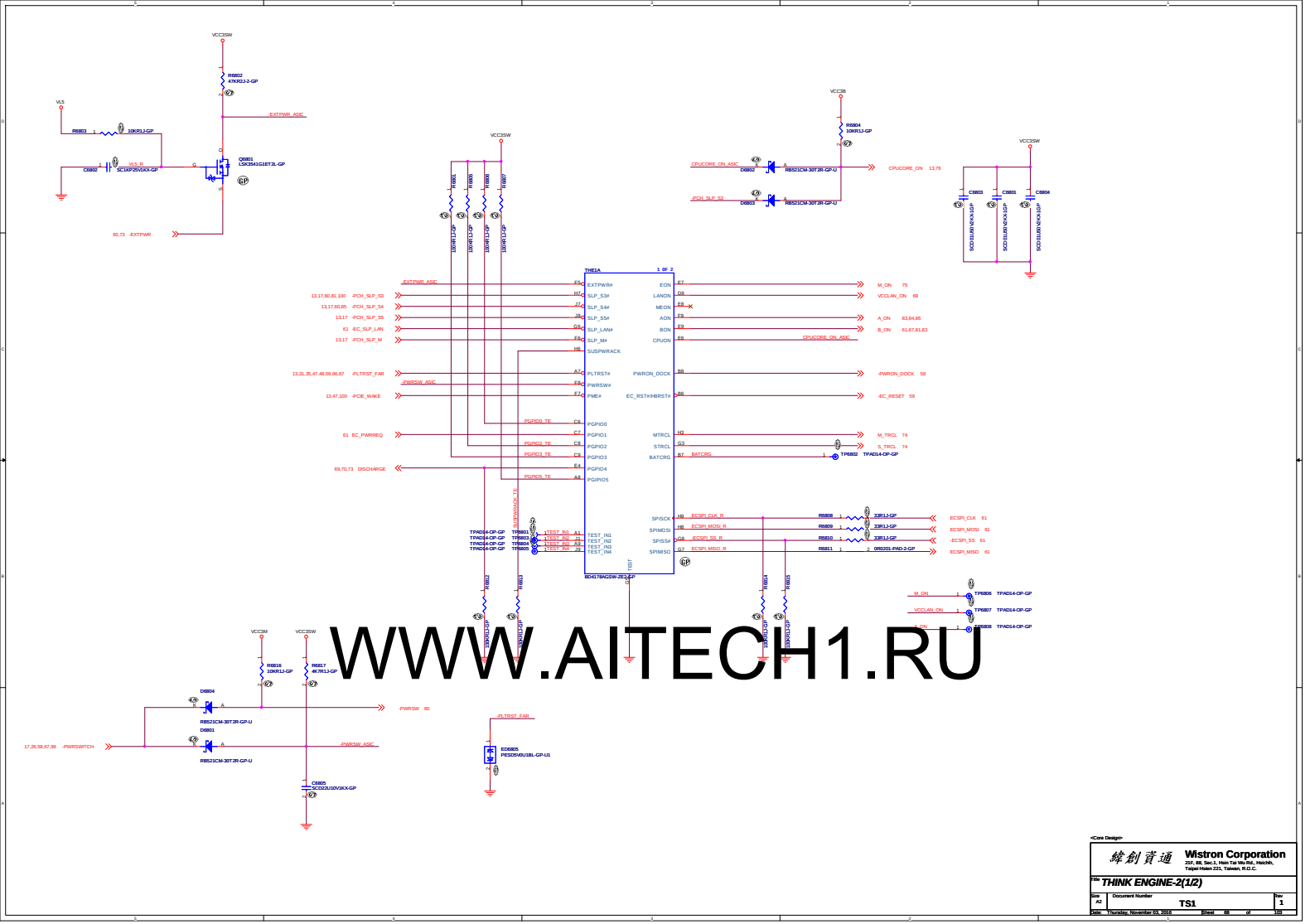
Title: SMBUS SWITCH/LPC DEBUG PORT

Size	Document Number	Rev
A3	TS1	1

Date: Thursday, November 03, 2016 Sheet 67 of 103



<Core Design>

緯創資通 Wistron Corporation

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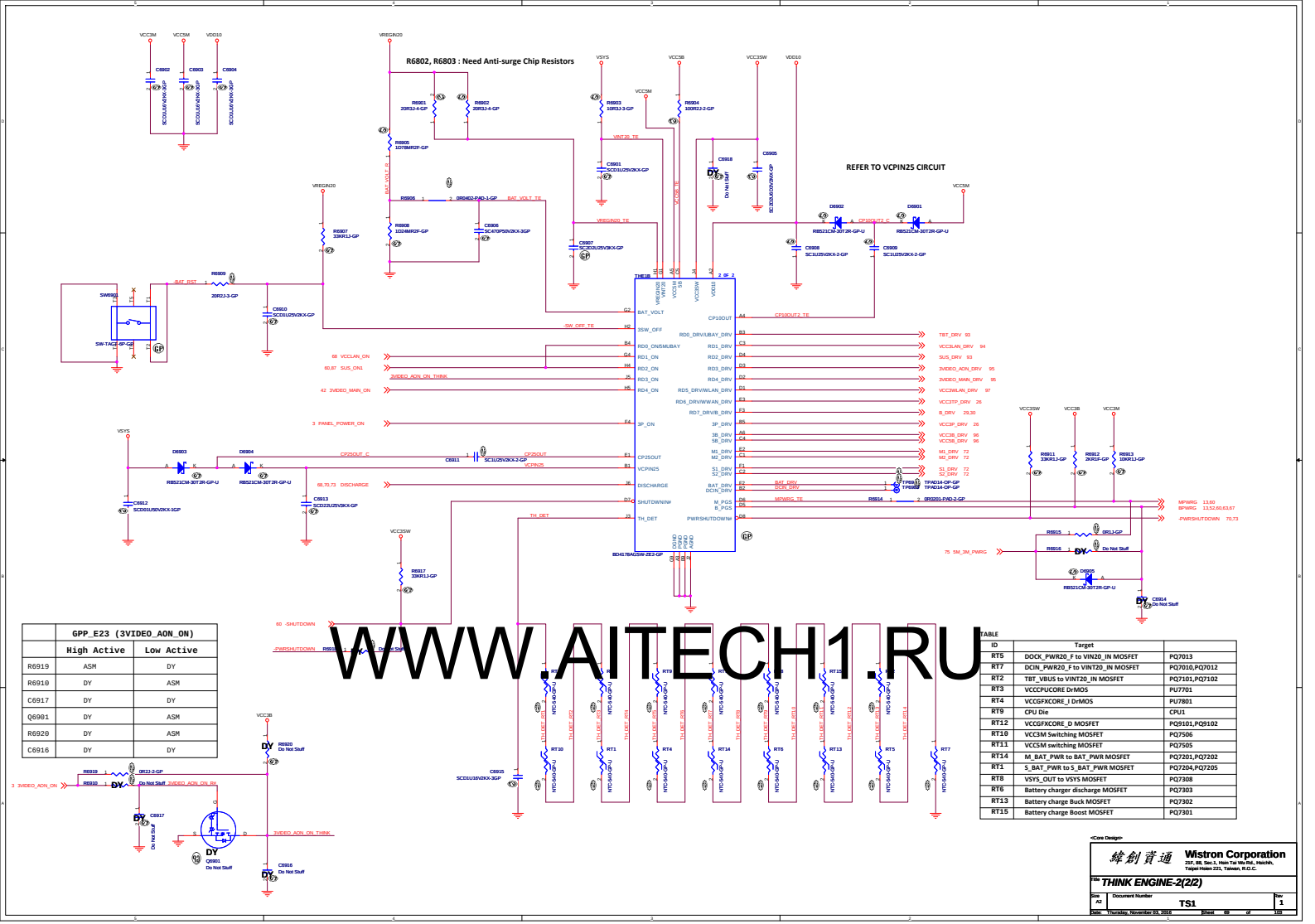
Title: THINK ENGINE-2(1/2)

Size	Document Number	Rev
A2	TS1	1

Date: Thursday, November 03, 2016 Sheet 68 of 100



	GPP_E23 (3VIDEO_AON_ON)	
	High Active	Low Active
R6919	ASM	DY
R6910	DY	ASM
C6917	DY	DY
Q6901	DY	ASM
R6920	DY	ASM
C6916	DY	DY

TABLE

ID	Target	
RT5	DOCK_PWR20_F to VIN20_IN MOSFET	PQ7013
RT7	DCIN_PWR20_F to VINT20_IN MOSFET	PQ7010,PQ7012
RT2	TBT_VBUS to VINT20_IN MOSFET	PQ7101,PQ7102
RT3	VCCCPUCORE DrMOS	PU7701
RT4	VCCGFXCORE_I DrMOS	PU7801
RT9	CPU Die	CPU1
RT12	VCCGFXCORE_D MOSFET	PQ9101,PQ9102
RT10	VCC3M Switching MOSFET	PQ7506
RT11	VCC5M switching MOSFET	PQ7505
RT14	M_BAT_PWR to BAT_PWR MOSFET	PQ7201,PQ7202
RT1	S_BAT_PWR to S_BAT_PWR MOSFET	PQ7204,PQ7205
RT8	VSYS_OUT to VSYS MOSFET	PQ7308
RT6	Battery charger discharge MOSFET	PQ7303
RT13	Battery charge Buck MOSFET	PQ7302
RT15	Battery charge Boost MOSFET	PQ7301

<Core Design>

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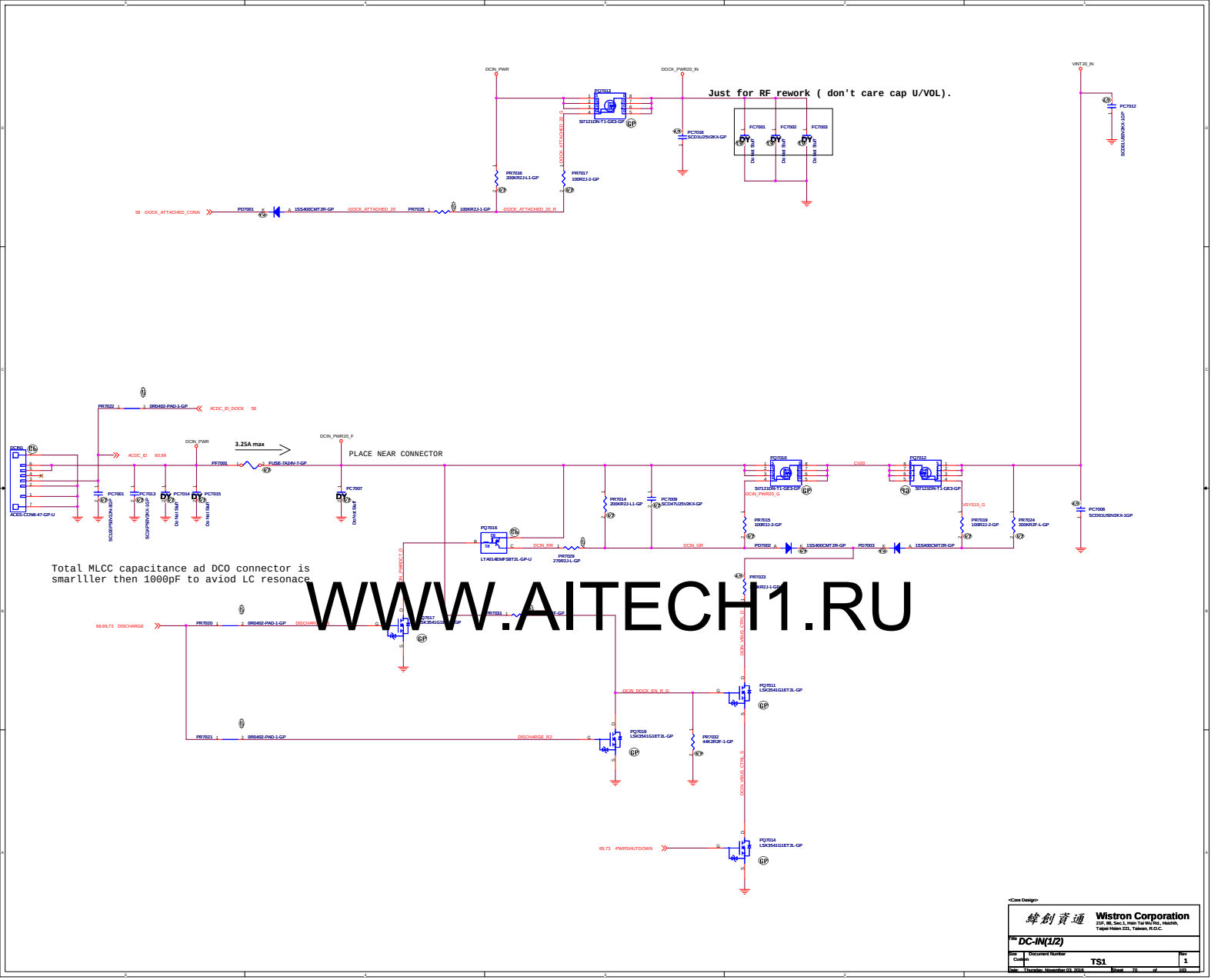
Title: THINK ENGINE-2(2/2)

Size	Document Number	Rev
A2	TS1	1

Date: Thursday, November 03, 2016 Sheet 68 of 100



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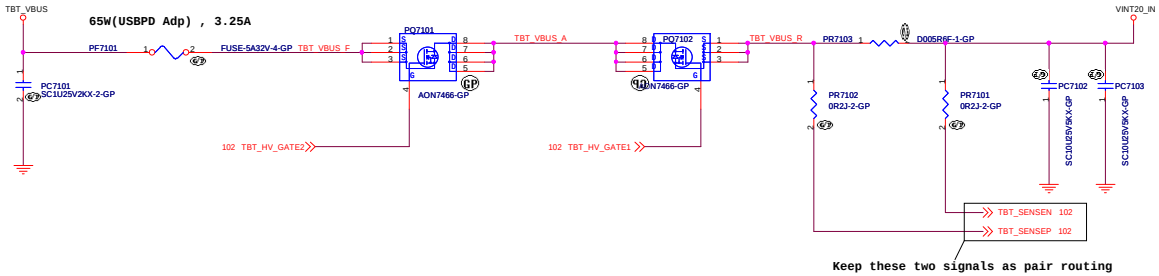
緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title: DC-IN(1/2)	
Size: Custom	Document Number: TS1
Rev: 1	
Date: Thursday, November 03, 2016	Sheet 20 of 103

PQ7101 and PQ7102

	Vendor	Vendor PN	Wistron PN
1st	AOS	AON7466	084.07466.0037
2nd	Rohm	RQ3E150GNA10	084.03150.0037



<Core Design>

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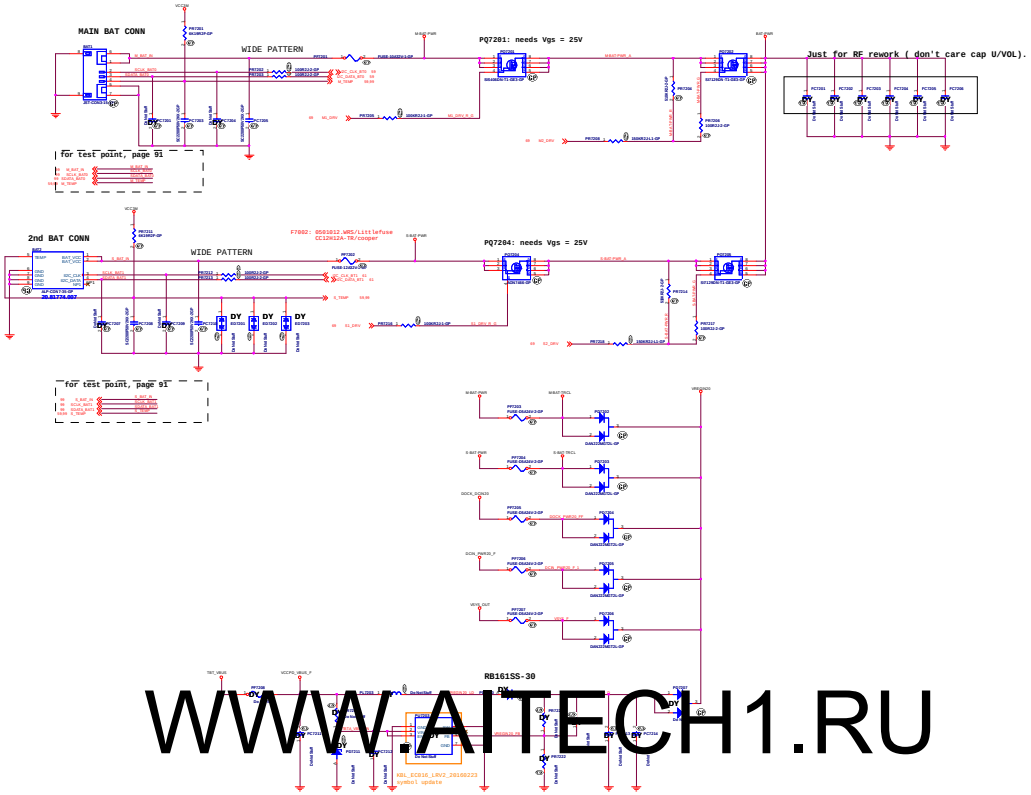
Taipei Hsien 221, Taiwan, R.O.C.

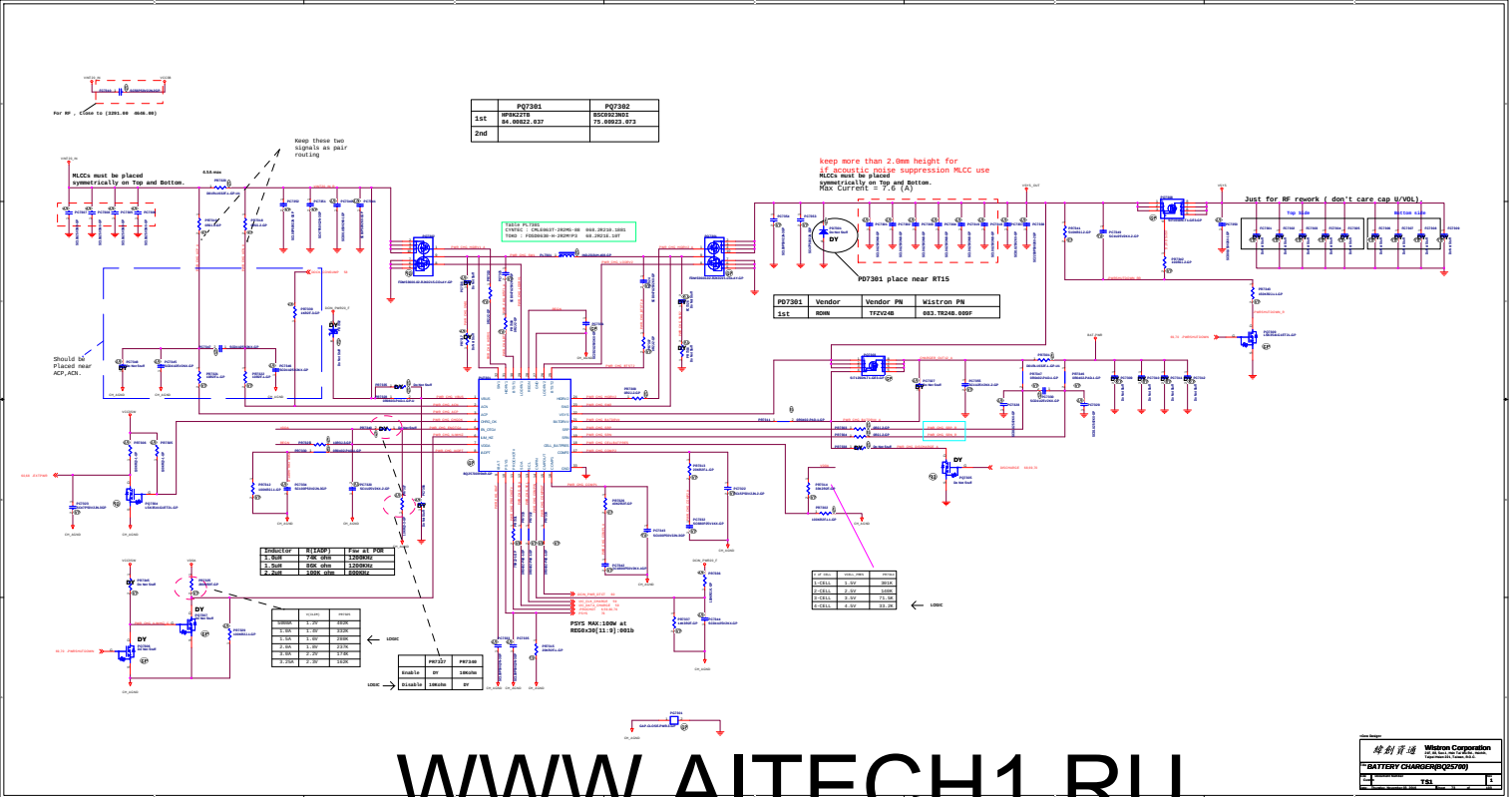
Title: DC-IN(2/2)

Size	Document Number	Rev
A3	TS1	1

Date: Thursday, November 03, 2016 Sheet 71 of 103



Wistron Corporation
BATTERY INPUT



	PQ7301	PQ7302
1st	MPBK227B 84.00822.037	RSC0923BDI 75.00823.073
2nd		

PD7301	Vendor	Vendor PN	Wistron PN
1st	ROHN	TFZV24B	083.TR24B.009F

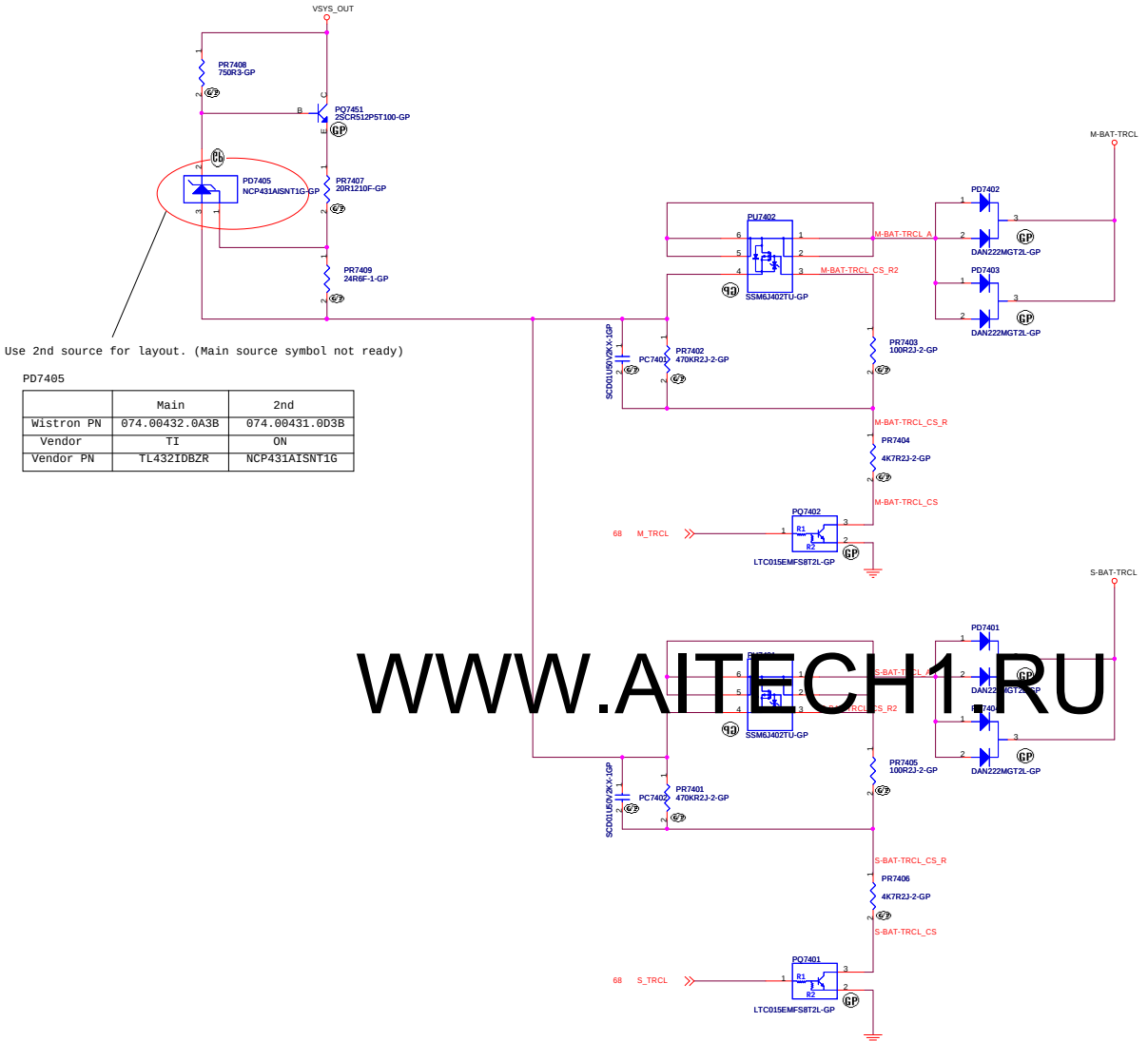
Inductor	R(IADP)	Fsw at PSM
1.5uH	74K ohm	1200KHz
1.5uH	65K ohm	1200KHz
2.2uH	100K ohm	800KHz

VIN(MAX)	VIN(MIN)	PSYS(W)
9000mV	7.2V	282K
9.0A	7.2V	332K
8.5A	7.2V	259K
7.6A	7.2V	237K
3.0A	7.2V	573K
2.25A	7.2V	343K

	PB7127	PB7340
Enable	DY	100uHm
Disable	100uHm	DY

# of Cells	VIN(L_ENT)	PSYS(W)
1-CELL	3.5V	301K
2-CELL	2.5V	146K
3-CELL	3.5V	71.5K
4-CELL	4.5V	33.2K

Wistron Corporation	
"BATTERY CHARGER(BQ25700)	
TS1	A



Use 2nd source for layout. (Main source symbol not ready)

PD7405

	Main	2nd
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Vendor	TI	ON
Vendor PN	TL432IDBZR	NCP431AISNT1G

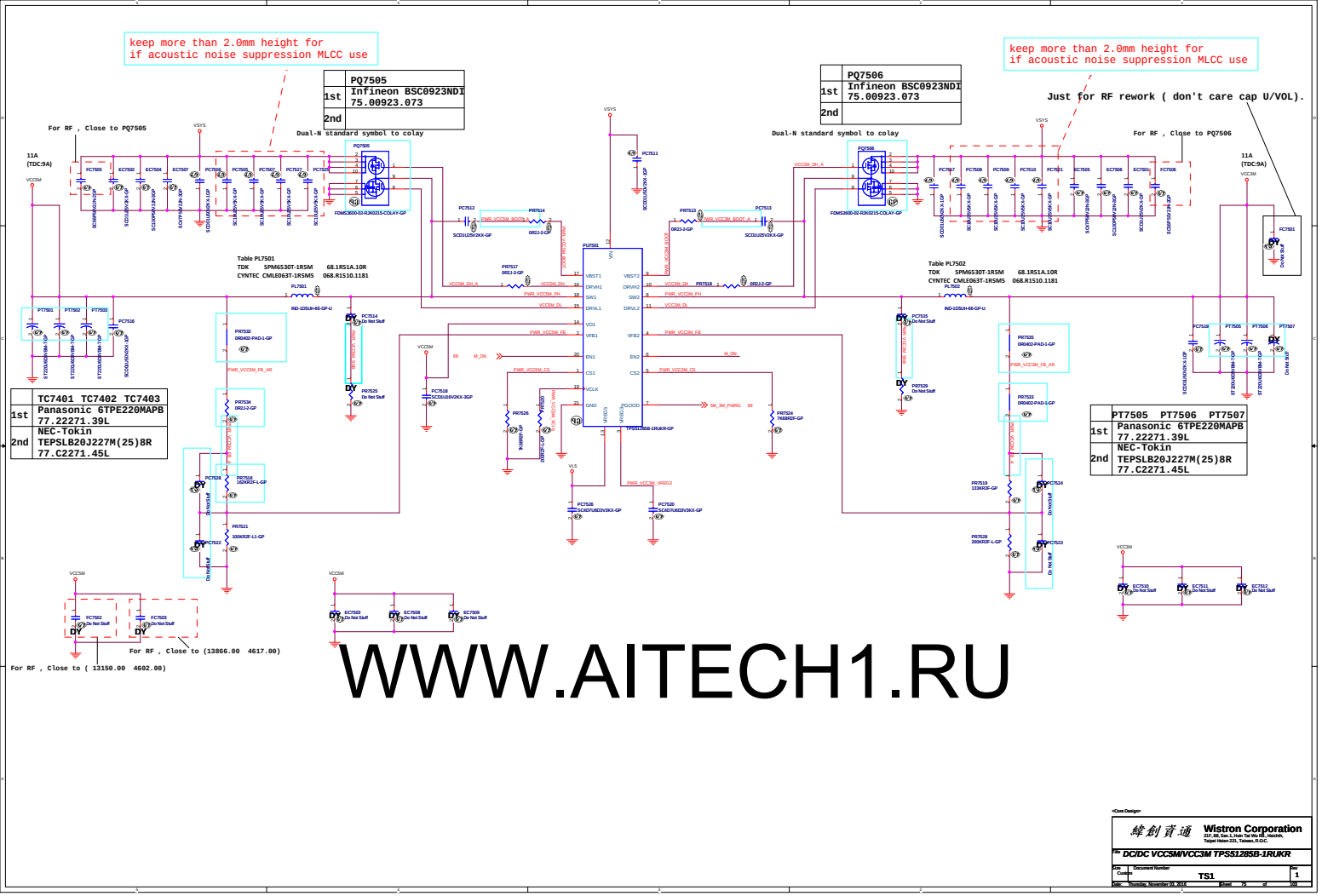
<Core Design>

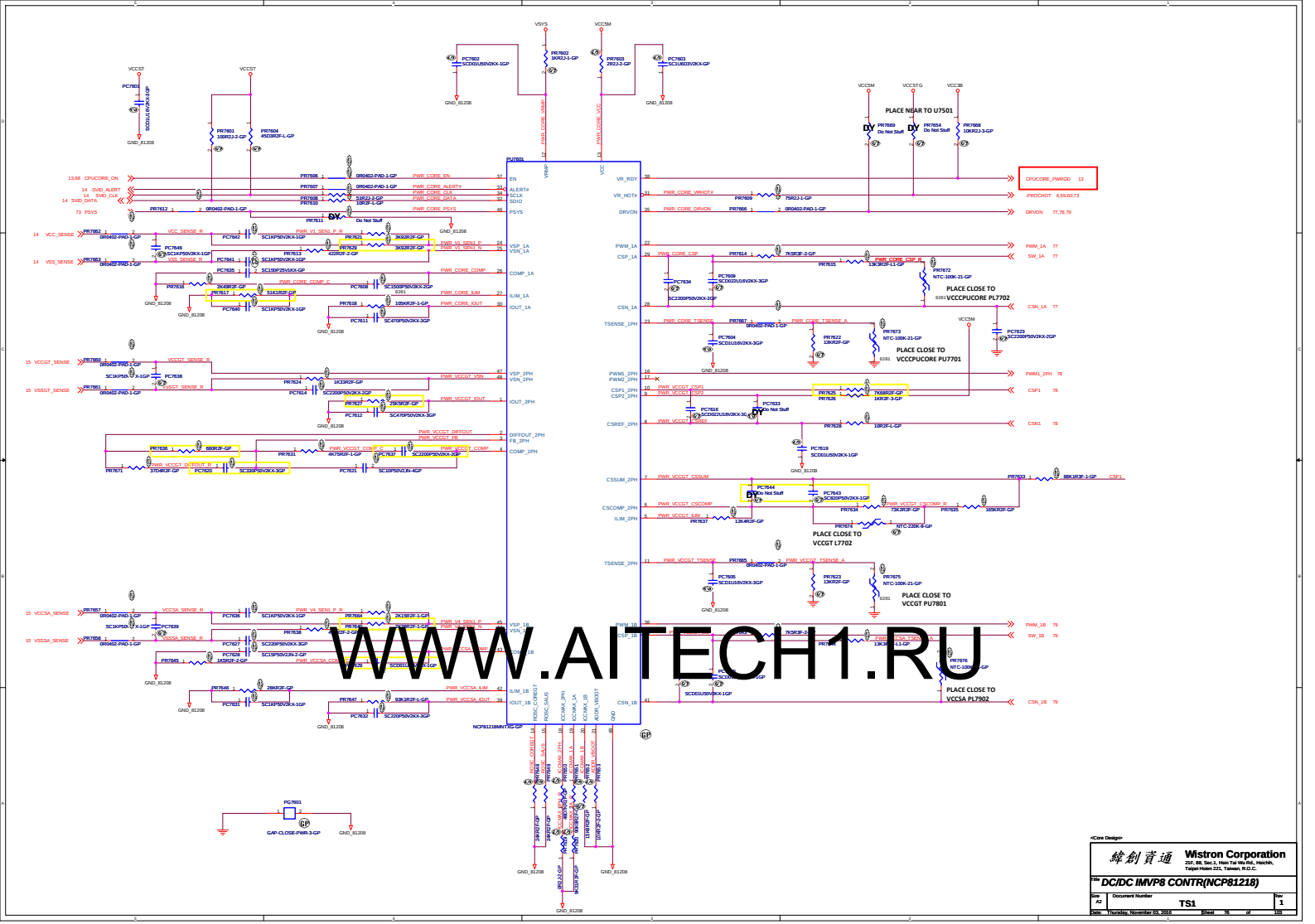
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title **CHARGER MONITOR**

Size: Custom | Document Number | Rev

Date: Thursday, November 03, 2016 | Sheet 74 of 103





MLCCs must be placed
symmetrically on Top and Bottom.

keep more than 2.0mm height for
if acoustic noise suppression MLCC use

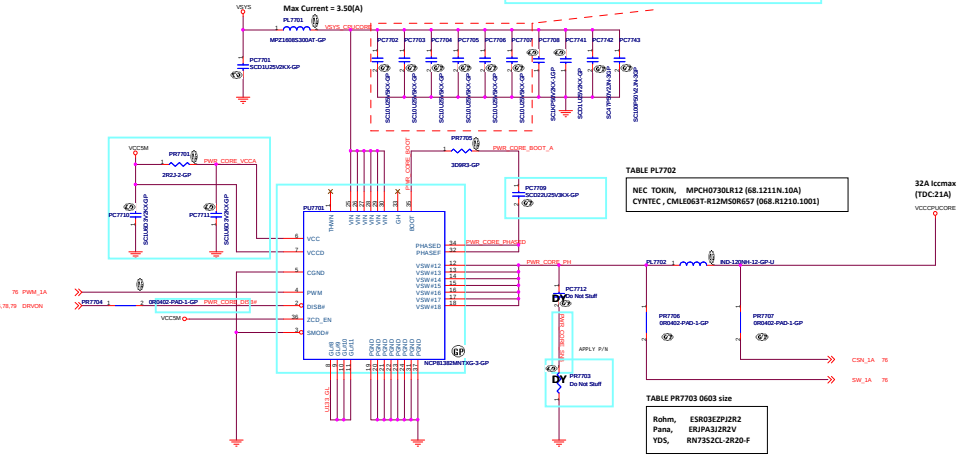
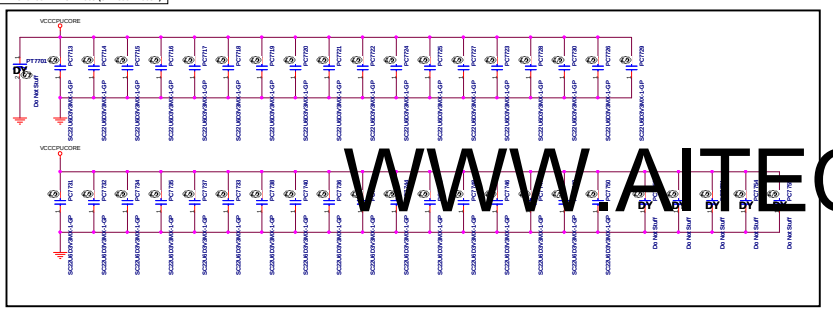


TABLE PR7703 0603 size

Rohm, ESR03EZPJ2R2
Pana, ERJPA3J2R2V
YDS, RN73S2CL-2R20-F

TABLE for PT7701

NEC TOKIN PSGB20E337M9 (80.3371V.A2L)
Panasonic ETPE330MA9L (No Wistron P/N)
KEMET T520B337M2R5ATE009 (077.C3371.0051)



22uF (0603) x 35 pcs
22uF (0603) x 5 pcs (DY)
330uF x 1 pcs (DY)

<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DC/DC VCCCPUCORE(NCP81382)

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Date: Friday, November 04, 2016 Sheet 77 of 100

keep more than 2.0mm height for
if acoustic noise suppression MLCC use

MLCCs must be placed
symmetrically on Top and Bottom.

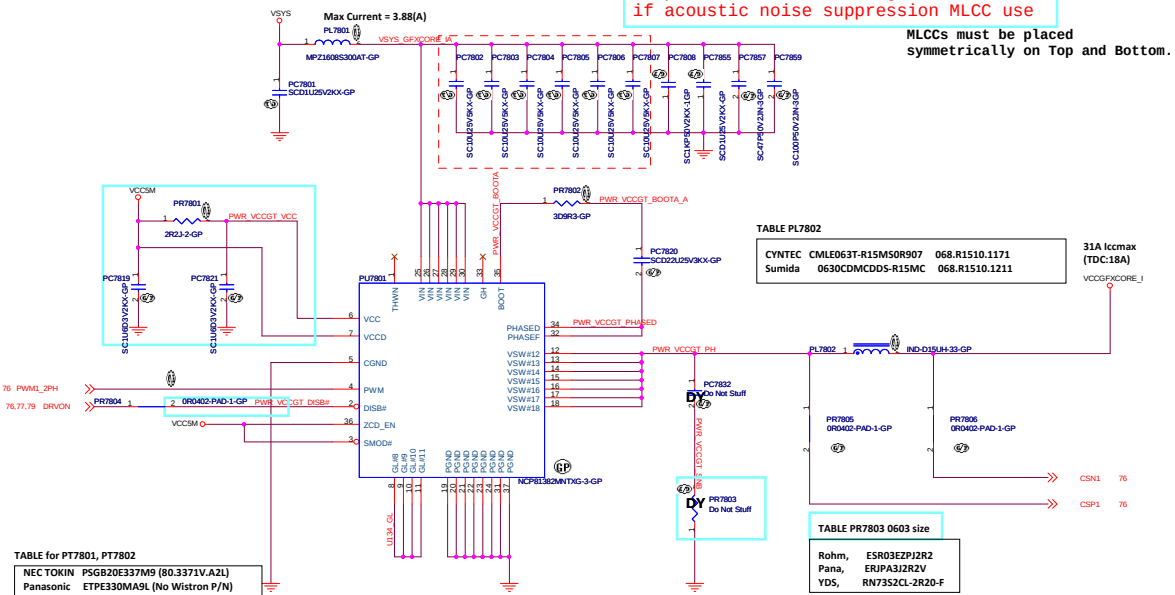


TABLE PL7802

CYNTEC	CMLE063T-R15MS0R907	068.R1510.1171
Sumida	0630CDMCDDS-R15MC	068.R1510.1211

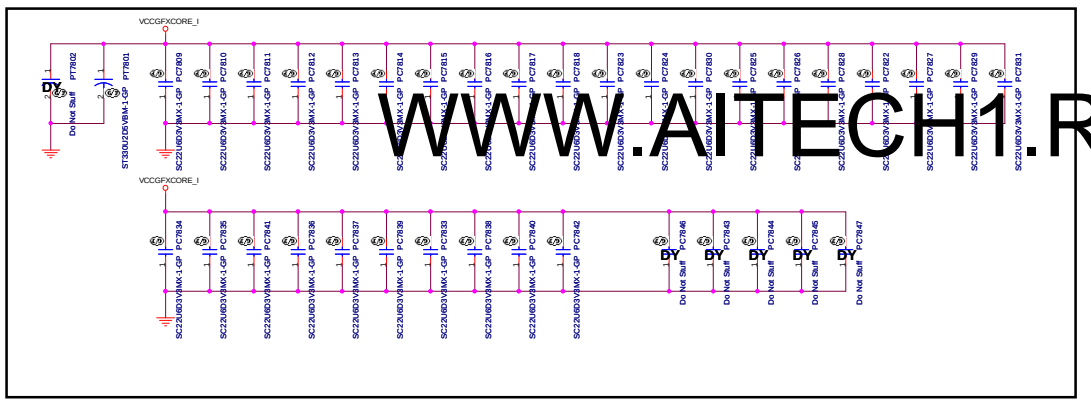
31A Iccmax
(TDC:18A)

TABLE PR7803 0603 size

Rohm,	ESR03EZPJ2R2
Pana,	ERJPA3J2R2V
YDS,	RN73S2CL-2R20-F

TABLE for PT7801, PT7802

NEC TOKIN	PSGB20E337M9 (80.3371V.A2L)
Panasonic	ETPE330MA9L (No Wistron P/N)
KEMET	T520B337M2R5ATE009 (077.C3371.0051)



22uF (0603) x 30 pcs
330uF x 1pcs
22uF (0603) x 5 pcs (DY)
330uF x 1 pcs (DY)

<Core Design>

緯創資通 Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: DC/DC VCCGFXCORE_I(NCP81382

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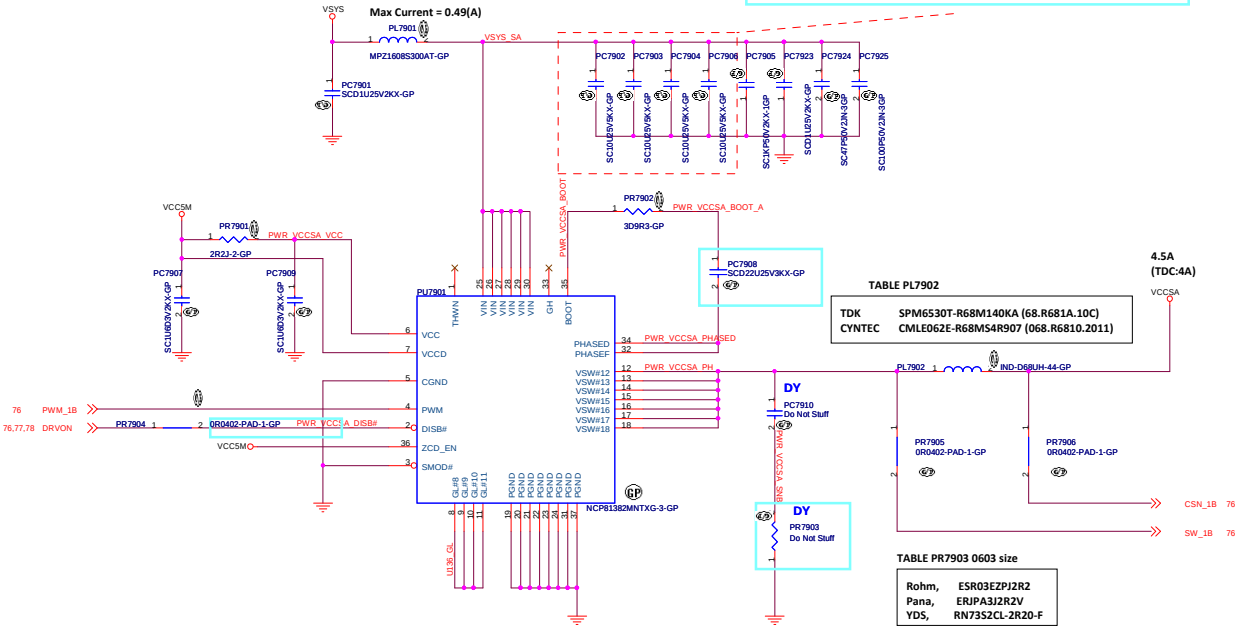
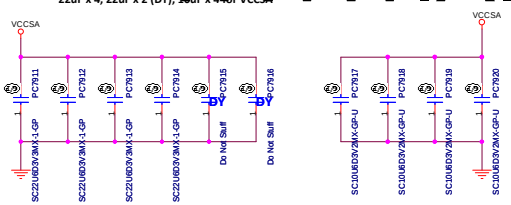
MLCCs must be placed
symmetrically on Top and Bottom.

keep more than 2.0mm height for
if acoustic noise suppression MLCC use



22uF x 4, 22uF x 2 (DY), 10uF x 4 for VCCSA



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Title: DC/DC VCCSA(NCP81380)

Size	Document Number	Rev
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Date: Thursday, November 03, 2016 Sheet 79 of 103

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<Core Design>

緯創資通 **Wistron Corporation**
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Taipei Hsien 221, Taiwan, R.O.C.

Title: *N/A*		
Size: A4	Document Number: TS1	Rev: 1
Date: Thursday, November 03, 2016	Sheet 80 of 103	

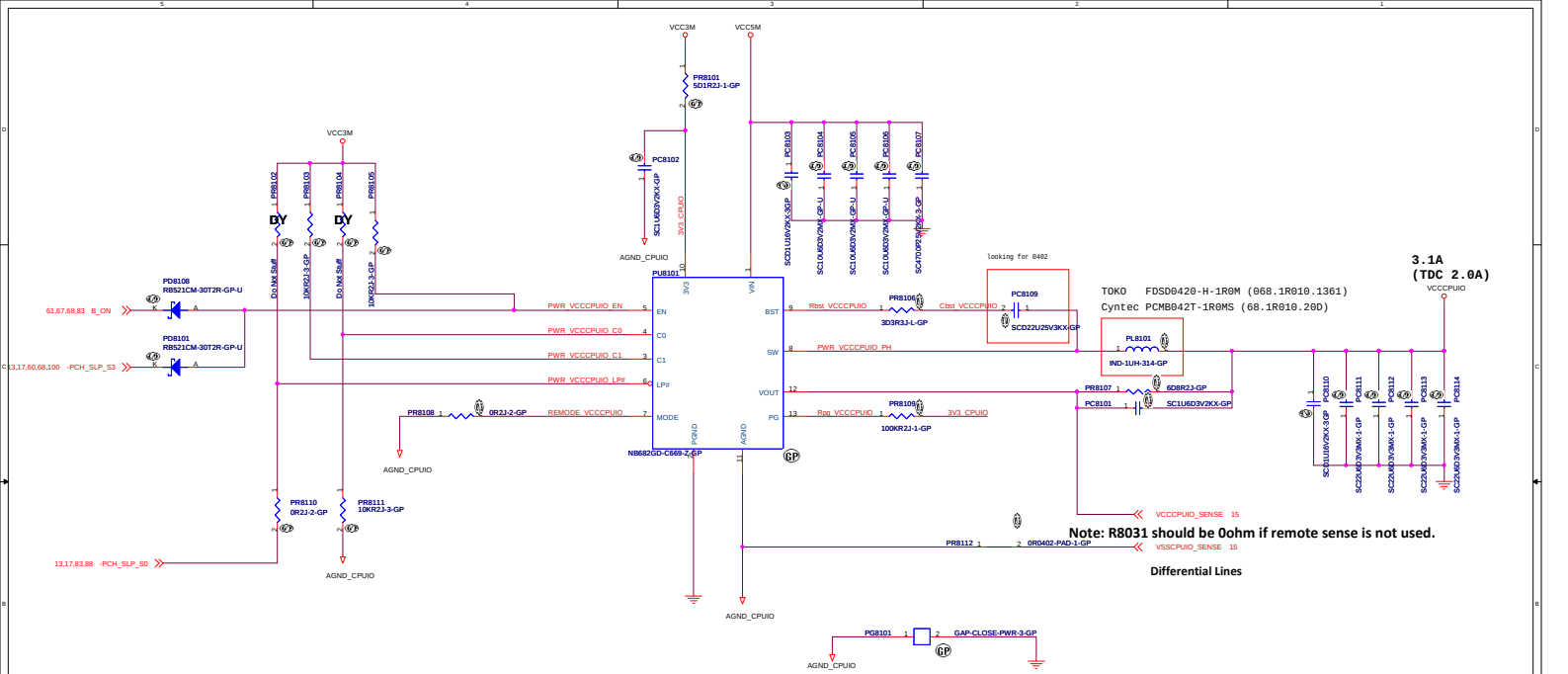
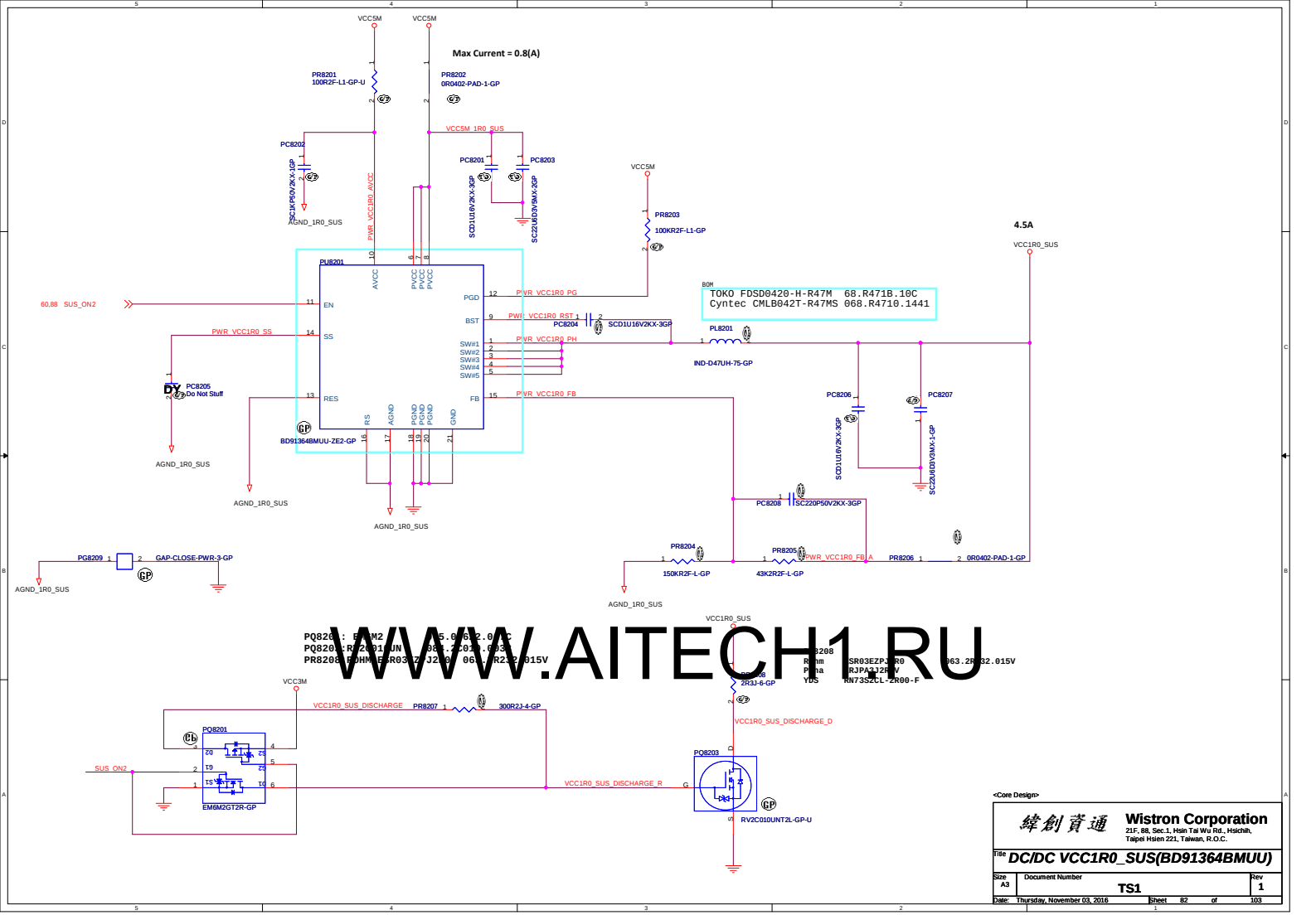


TABLE : NB682 MODE M1 (0 to GND)

LP#	C1	C0	VOUT
0	X	X	0.00V
1	0	0	0.850V
1	0	1	0.875V
1	1	0	0.950V
1	1	1	0.975V

<Core Design>

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	DC/DC VCCCPUIO(NB682)
Size: Custom	Document Number: TS1
Rev	1
Date: Thursday, November 03, 2016	Sheet 81 of 103



<Core Design>
緯創資通 Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: DC/DC VCC1R0_SUS(BD91364BMUU)

Size	Document Number	Rev
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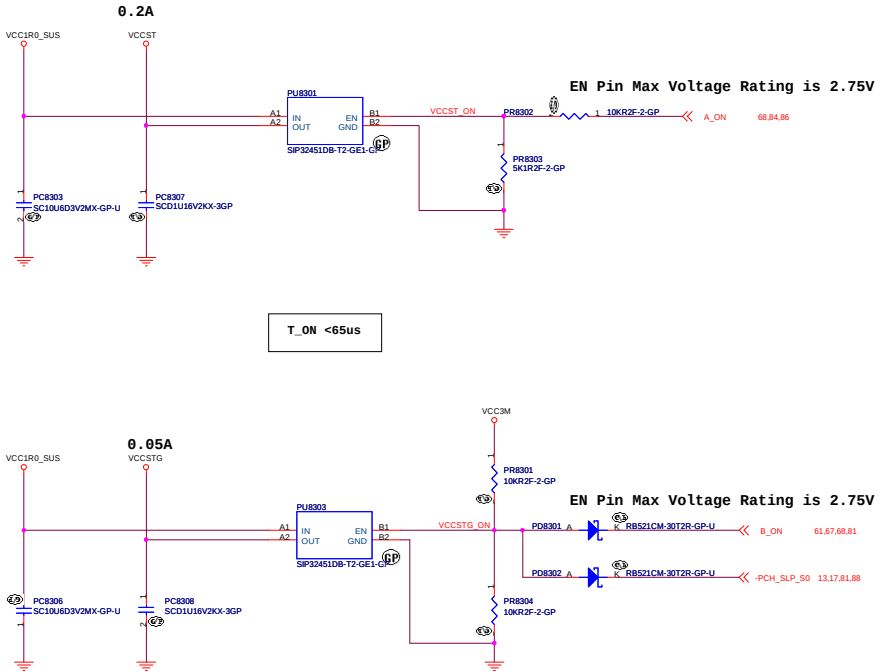
Date: Thursday, November 03, 2016 Sheet 82 of 103



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緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: LOAD SW VCCST & VCCSTG

Size	Document Number	Rev
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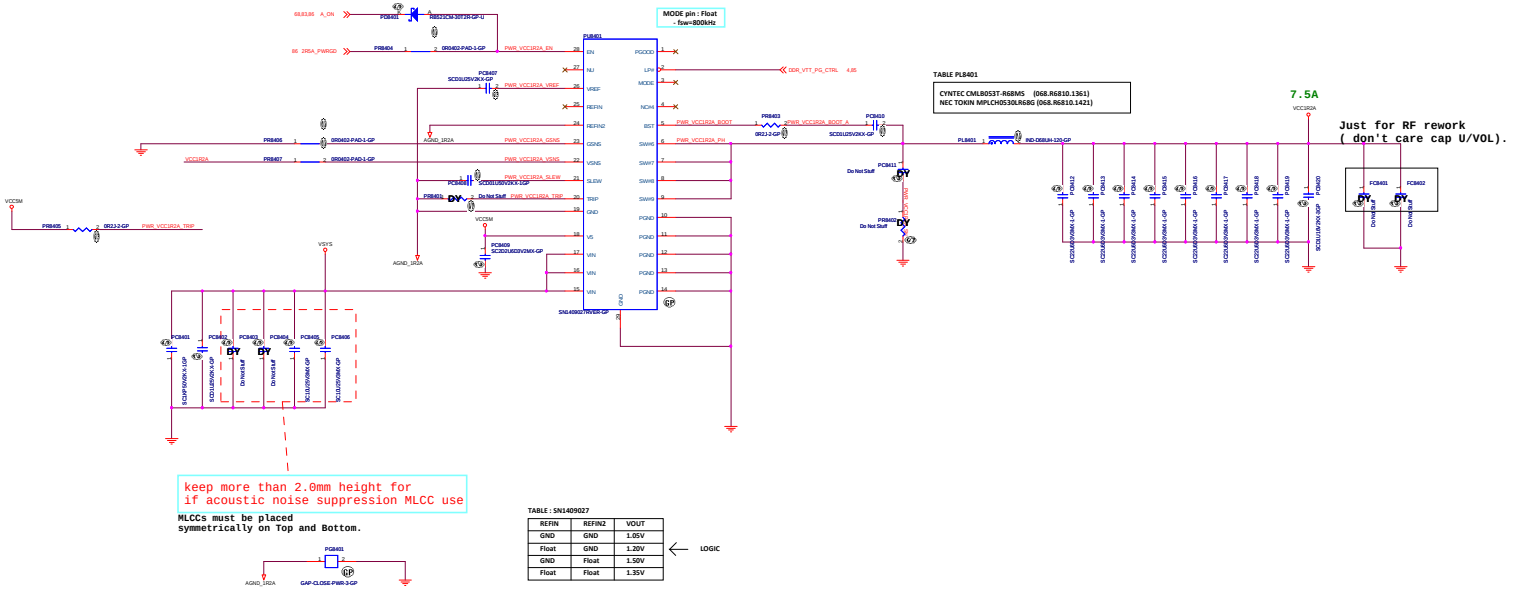

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Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.
Title: DC/DC VCC1R2A
Size: C | Custom | Document Number | Rev
Date: Thursday, November 03, 2016 | Sheet pg of 103

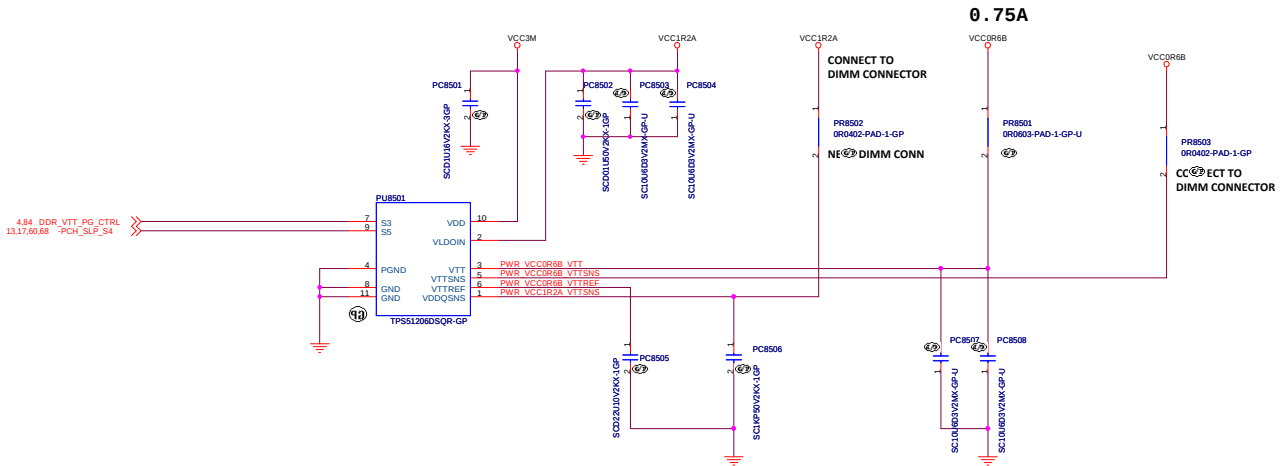

TABLE: TPS51206

S3	S5	VTT	VTTREF
High	High	ON	ON
Low	High	OFF(High-Z)	ON
Low	Low	OFF(Discharge)	OFF(Discharge)

<Core Design>

緯創資通 Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: DC/DC VCC0R6B

Size: A3 | Document Number | Rev

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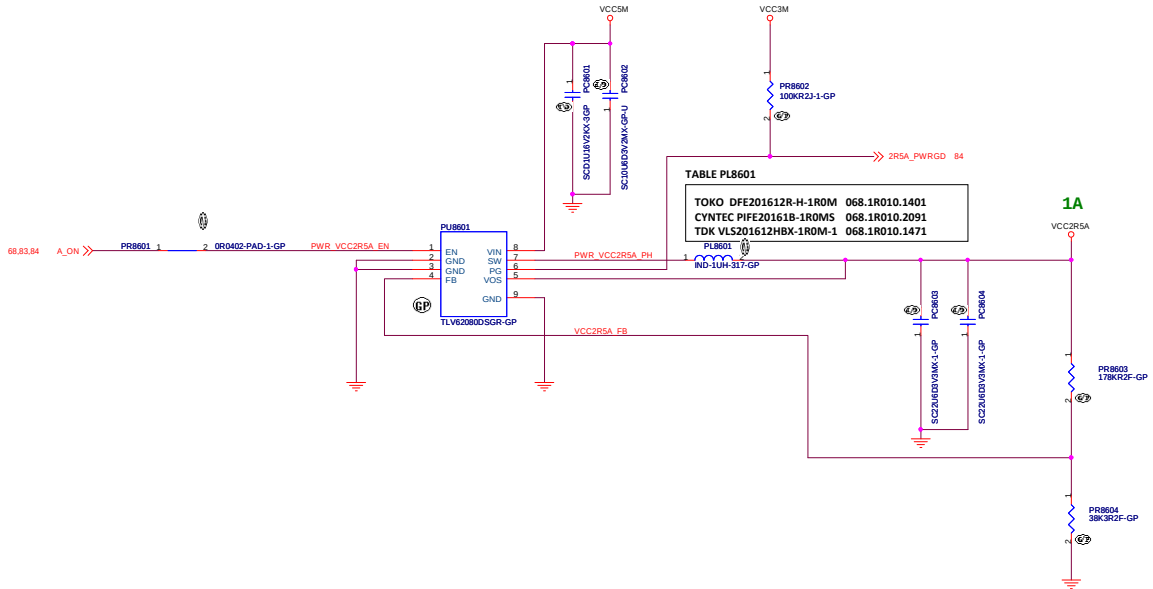

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Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: DC/DC VCC2R5A

Size: A3 | Document Number | Rev

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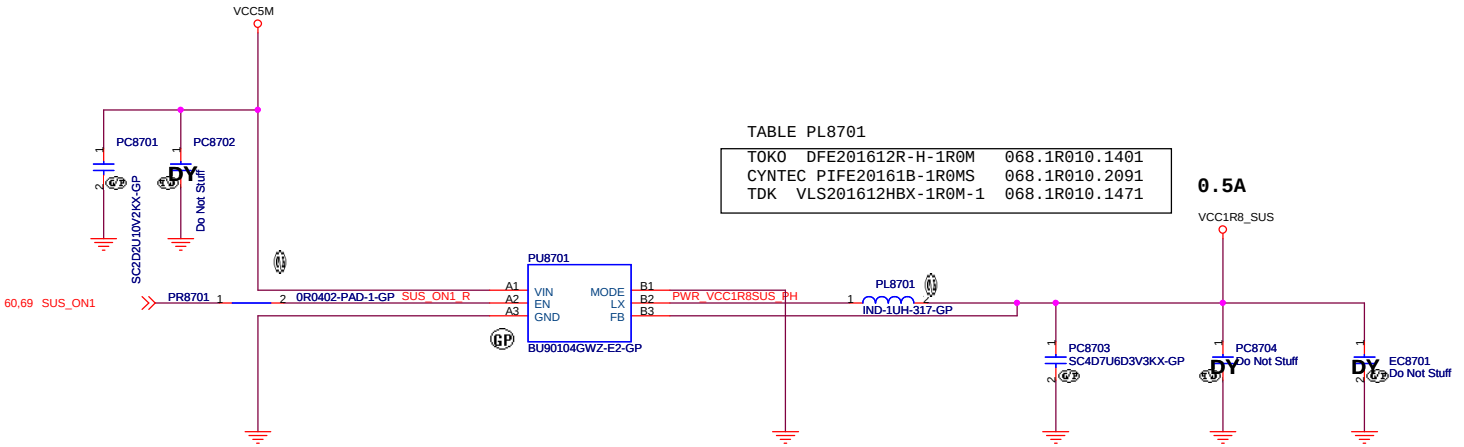

TABLE PL8701

TOKO	DFE201612R-H-1R0M	068.1R010.1401
CYNTEC	PIFE20161B-1R0MS	068.1R010.2091
TDK	VLS201612HBX-1R0M-1	068.1R010.1471

0.5A

<Core Design>

緯創資通 **Wistron Corporation**
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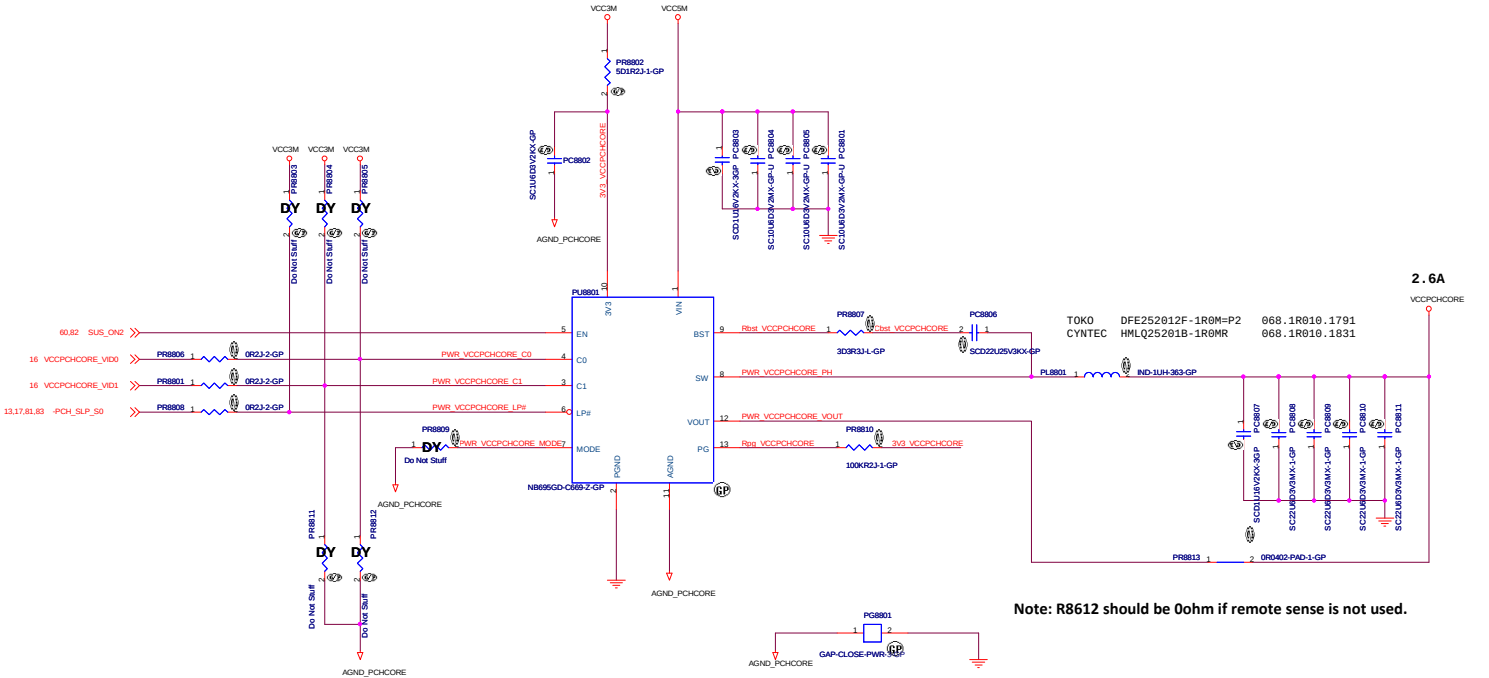
Title	***DC/DC VCC1R8_SUS***		
Size: Custom	Document Number: **TS1**		Rev: **1**
Date: Thursday, November 03, 2016	Sheet 87 of 103		



Note: R8612 should be 0ohm if remote sense is not used.

TABLE : NB682 MODE M2 (Float) - ES

LP#	C1	C0	VOUT	
0	X	X	0.700V	← SLP_S0#
1	0	0	0.850V	
1	0	1	0.900V	
1	1	0	0.950V	
1	1	1	1.000V	← DEFAULT

<Core Design>

緯創資通 **Wistron Corporation**
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Taipei Hsien 221, Taiwan, R.O.C.

Title: *086_DC/DC VCCPCHCORE(NB682)*

Size	Document Number	Rev
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<Core Design>

緯創資通

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Taipei Hsien 221, Taiwan, R.O.C.

Title	***BLANK***	
Size: A	Document Number: **TS1**	Rev: **1**
Date: Thursday, November 03, 2016	Sheet 89 of 103	

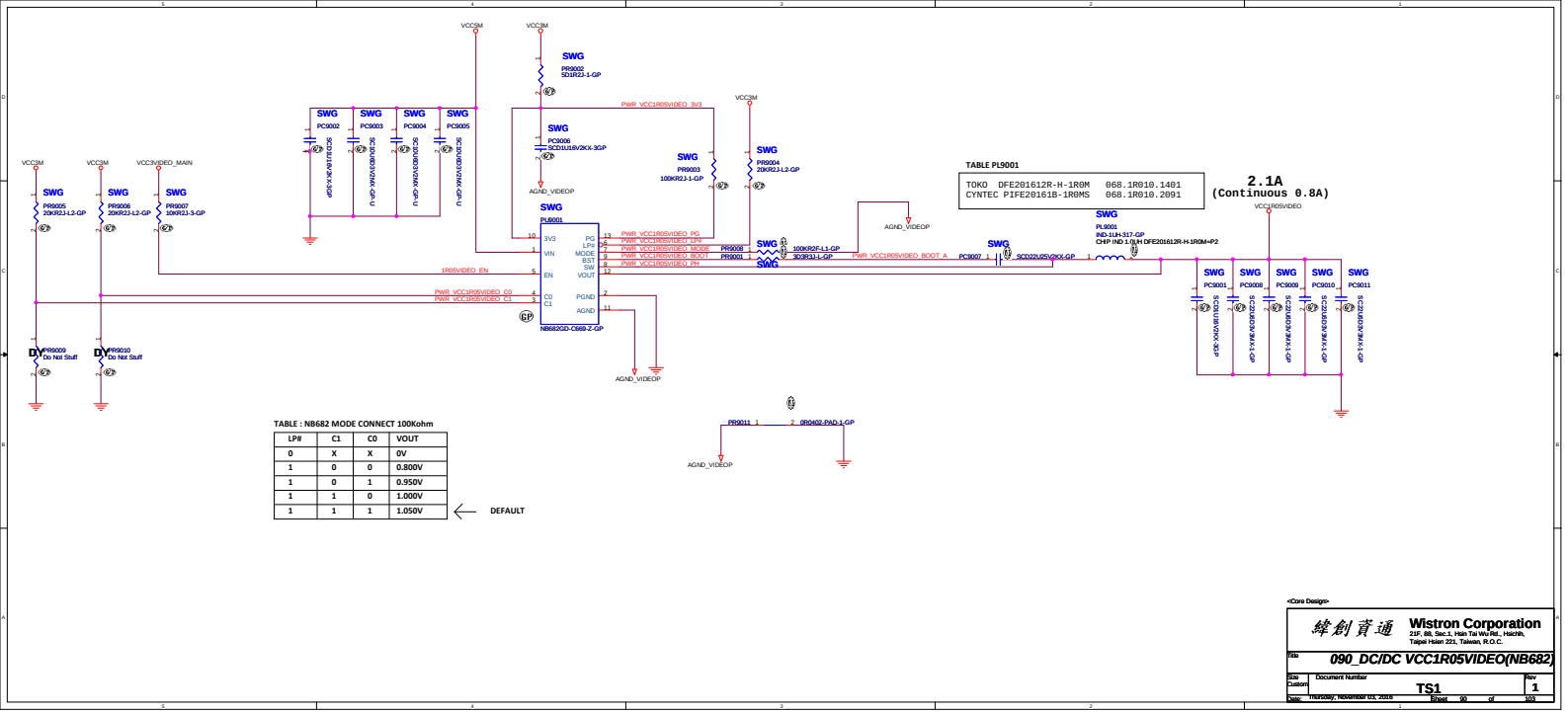


TABLE PL9001

TOKO DFE201612R-H-1R0M	068.1R010.1401
CYNTEC PIFE20161B-1R0MS	068.1R010.2091

2.1A (Continuous 0.8A)

TABLE : NB682 MODE CONNECT 100Kohm

LP#	C1	C0	VOUT
0	X	X	0V
1	0	0	0.800V
1	0	1	0.950V
1	1	0	1.000V
1	1	1	1.050V ← DEFAULT

<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: 090_DC/DC VCC1R05VIDEO(NB682)

Size: Custom | Document Number: TS1 | Rev: 1

Date: Thursday, November 04, 2010 | Sheet 90 of 103

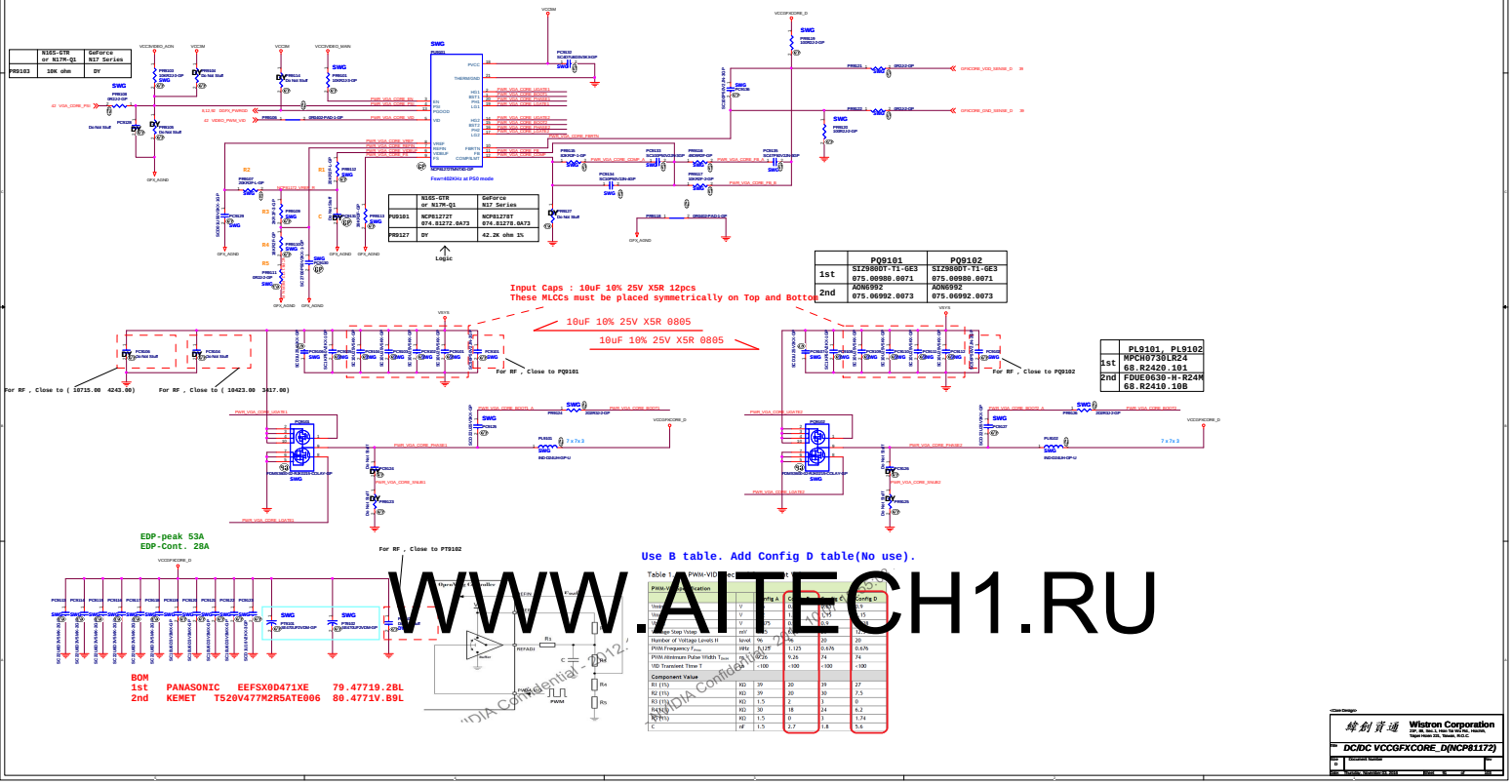
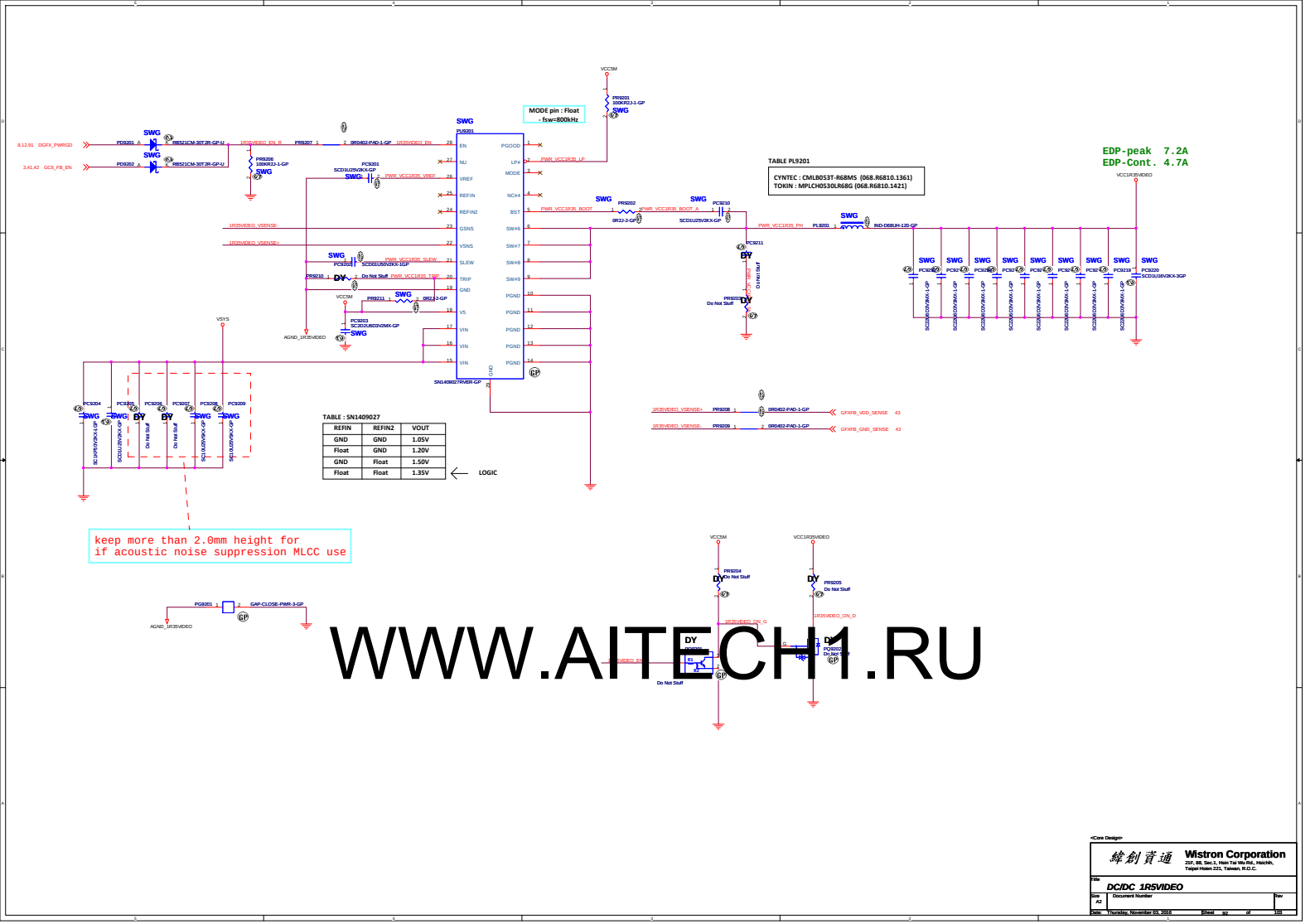


Table 1 PWM-VID Feature		Config A	Config B	Config C	Config D
Vboot	V			0	1.5
Vmax	V			1.1	1.515
Vmin	V			0.5	0.5
Voltage Step Vstep	mV	5	5	5	5
Number of Voltage Levels N	level	96	176	120	201
PWM Frequency F_{sw}	MHz	1.125	1.125	0.676	0.676
PWM Minimum Pulse Width T_{pwm}	ns	9.26	9.26	74	74
VID Transient Time T		<100	<100	<100	<100
Component Value					
R1 (1%)	KΩ	39	20	39	27
R2 (1%)	KΩ	39	20	30	7.5
R3 (1%)	KΩ	1.5	2	3	0
R4 (1%)	KΩ	30	16	24	6.2
R5 (1%)	KΩ	1.5	0	3	1.74
C	nF	1.5	2.7	1.8	5.6

Wistron Corporation	緯創資通
DC/DC VCCGFXCORE_D(NCP81172)	
Size: D	Document Number:
Date: Tuesday, November 06, 2012	Sheet 36 of 48



<Core Design>
緯創資通 Wistron Corporation
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Title: DC/DC 1R5VIDEO

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A2		

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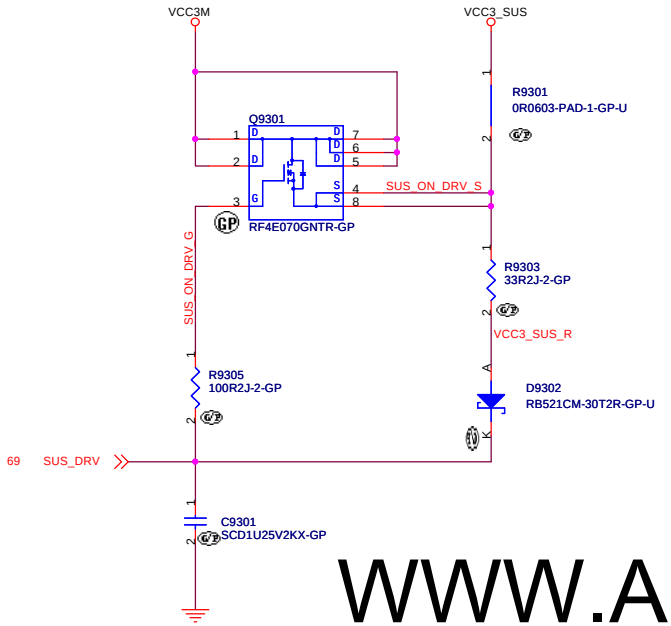
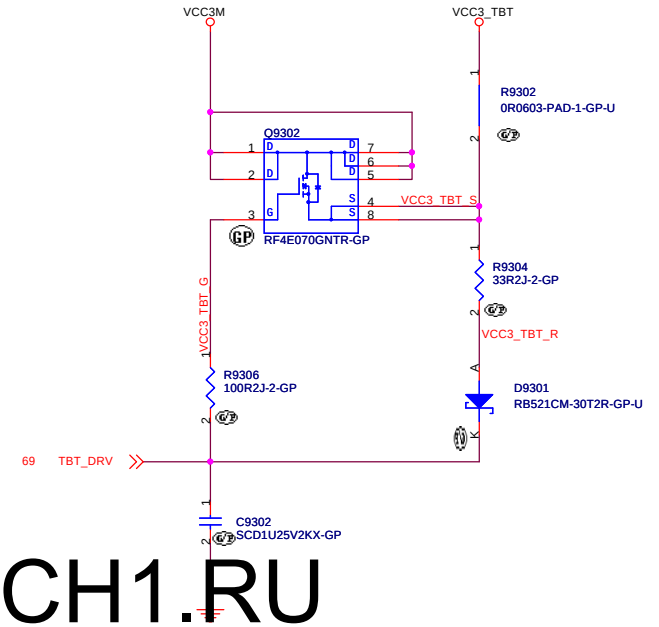
Q9301 Q9302		
Vendor	Venor PN	Wistron PN
Rohm	RF4E070GN (1st source)	084.4E070.0037
Fairchild	FDMA7672 (2nd source)	084.07672.M001

0.8A



1A



<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: LOAD SW PCH SUS/TRACK POINT

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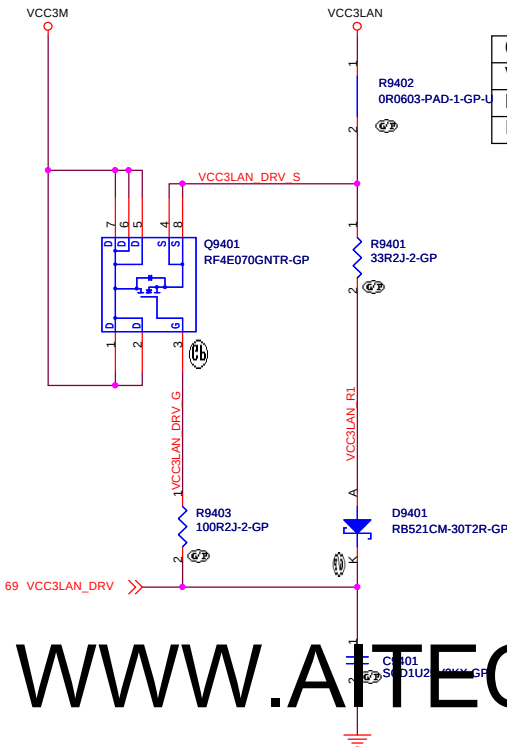
0.5A



Q9401		
Vendor	Venor PN	Wistron PN
Rohm	RF4E070GN (1st source)	084.4E070.0037
Fairchild	FDMA7672 (2nd source)	084.07672.M001

<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: LOAD SW LAN

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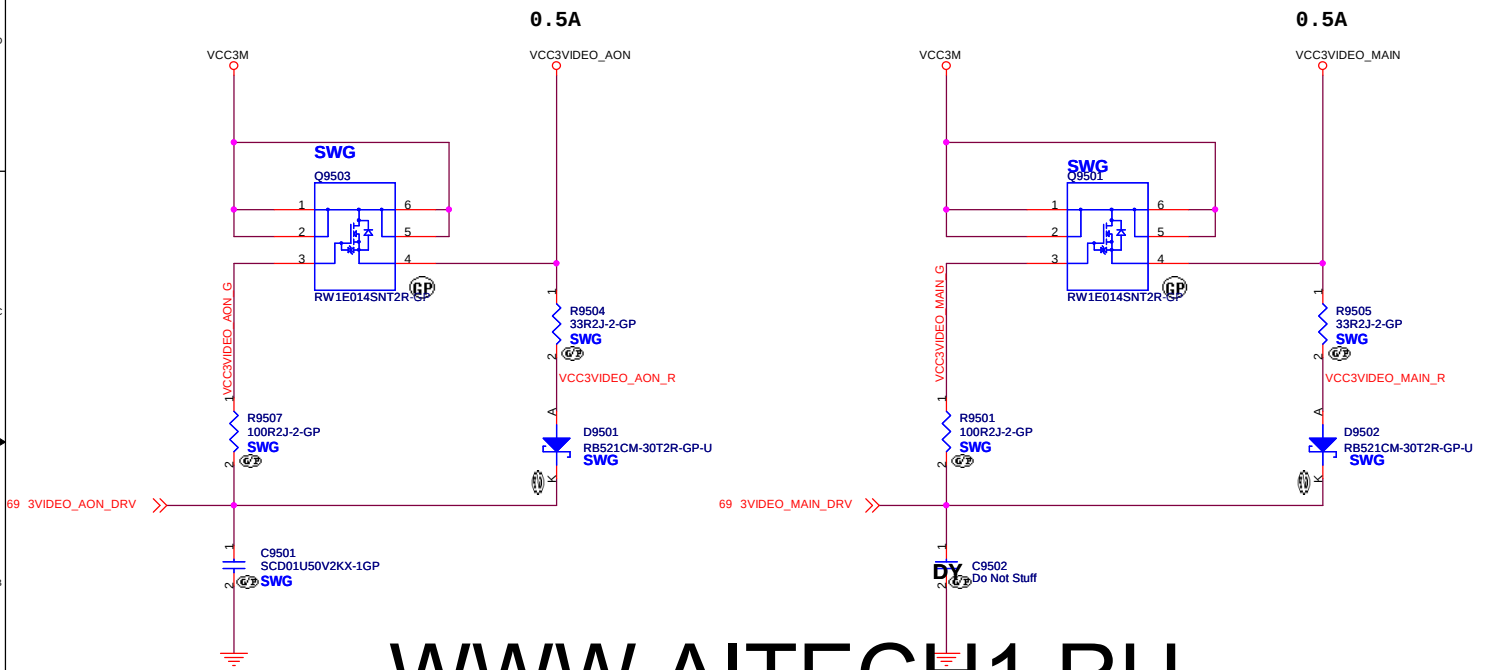

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緯創資通 **Wistron Corporation**
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Taipei Hsien 221, Taiwan, R.O.C.

Title: ***LOAD SW VIDEO***

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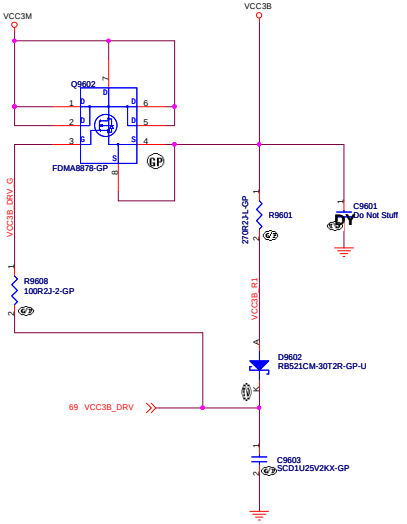
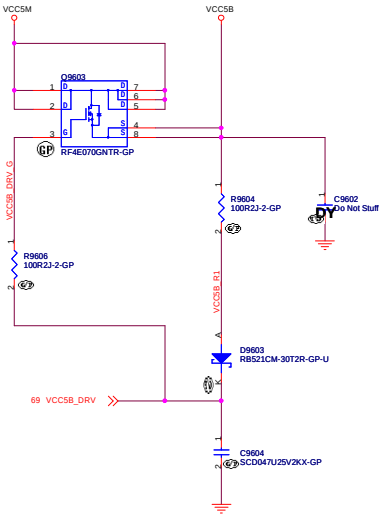
Q9602
FDMA8878 Fairchild 84.08878.030
SiA462DJ Vishay 084.00462.003D

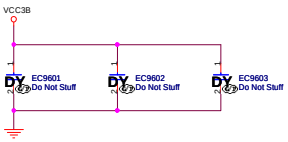
Q9603		
Vendor	Venor PN	Wistron PN
Rohm	RF4E070GN (1st source)	084.4E070.0037
Fairchild	FDMA7672 (2nd source)	084.07672.M001

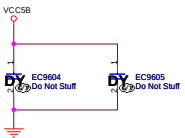
8.5A Peak
6.0A Cont.



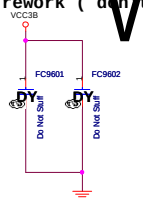
3.5A







Just for RF rework (don't care lab 0/VOA)



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緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: LOAD SW B

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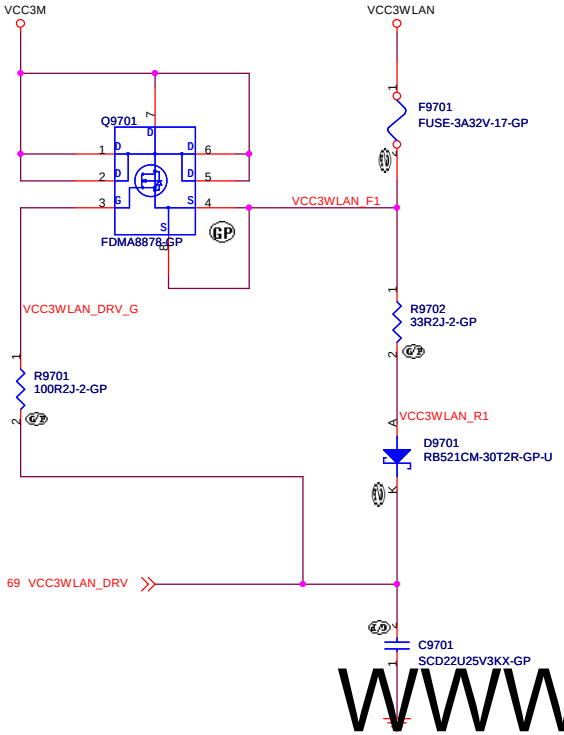
2.5A peak
1.1A Cont



Q9701
1st : Fairchild FDMA8878 84.08878.030
2nd : Vishay SiA462DJ 084.00462.003D

<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: LOAD SW WLAN

Size: A4 | Document Number: TS1 | Rev: 1

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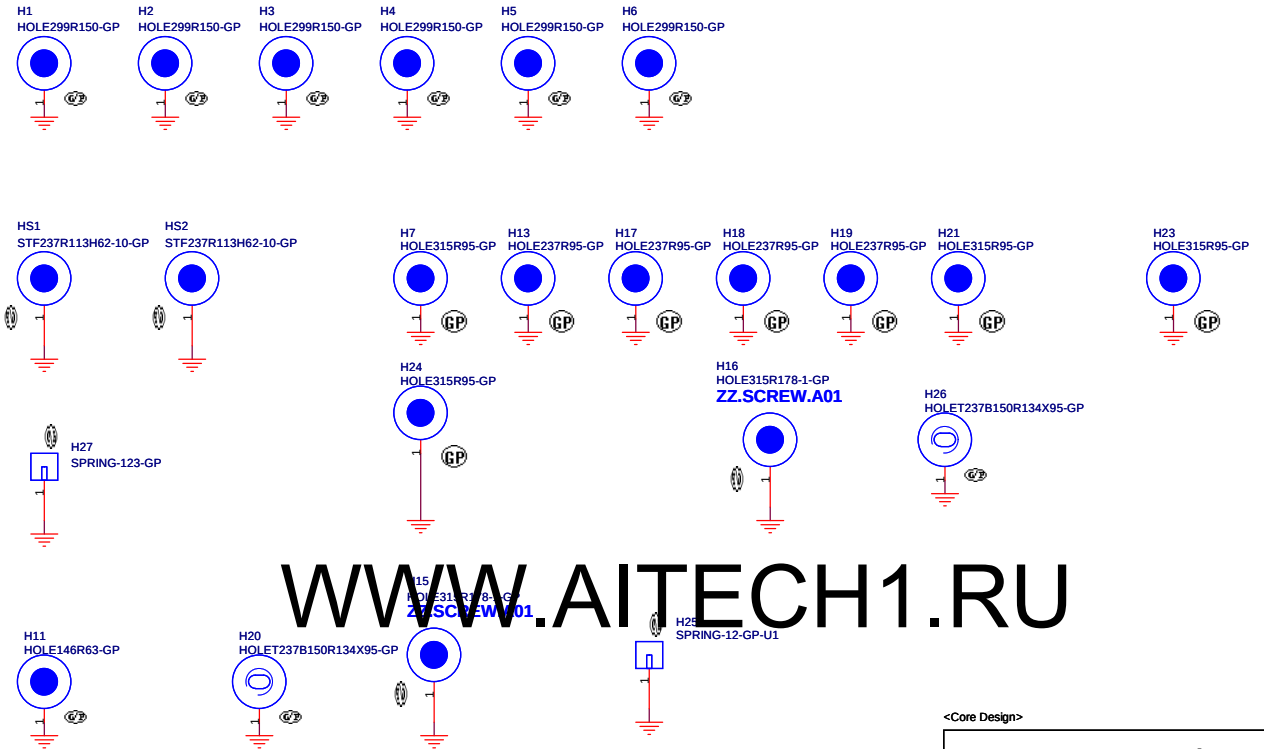

<Core Design>

緯創資通 **Wistron Corporation**
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Taipei Hsien 221, Taiwan, R.O.C.

Title: ***PTH FOR SCREW HOLES***

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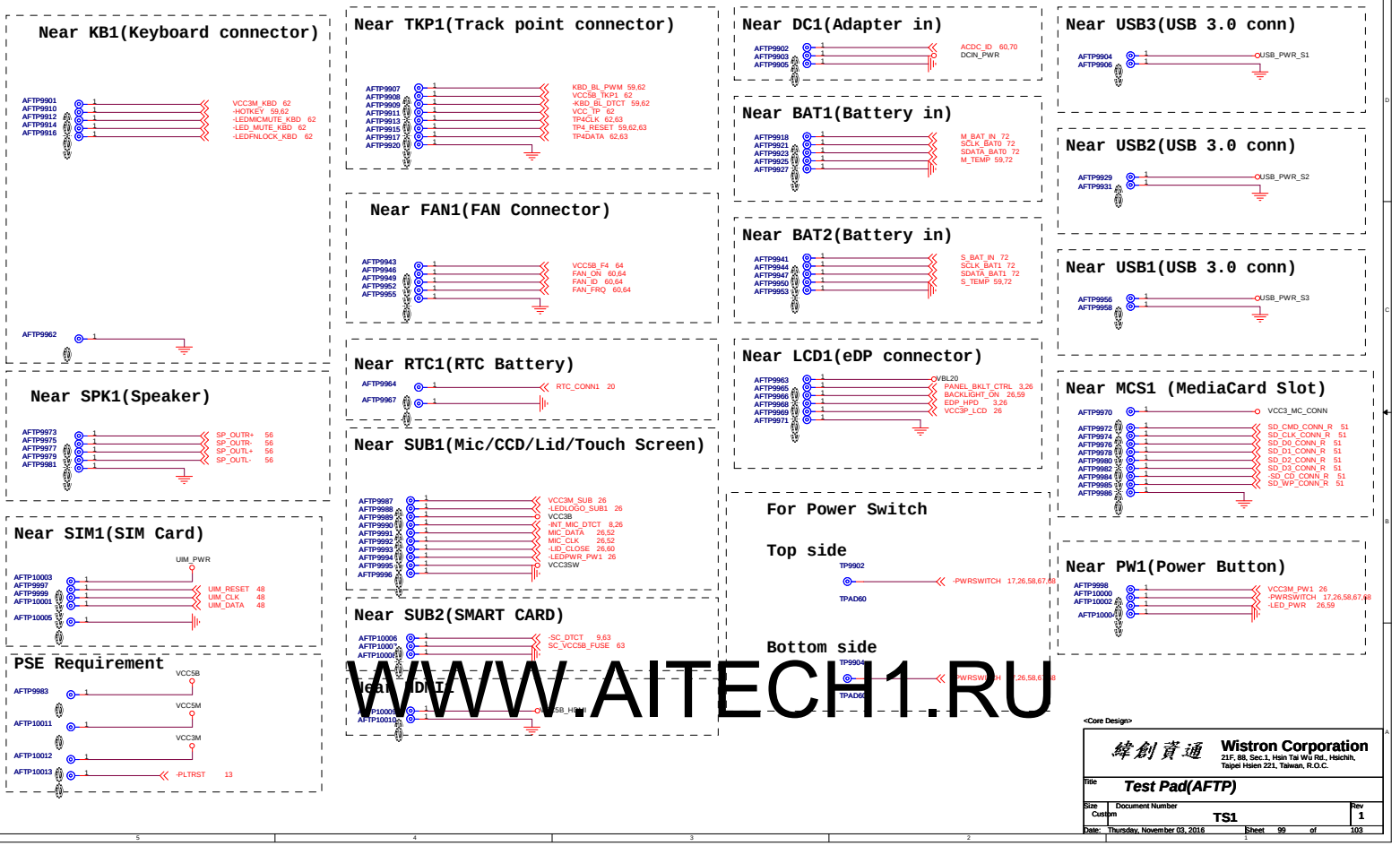

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緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Test Pad(AFTP)

Size: Custom | Document Number: TS1 | Rev: 1

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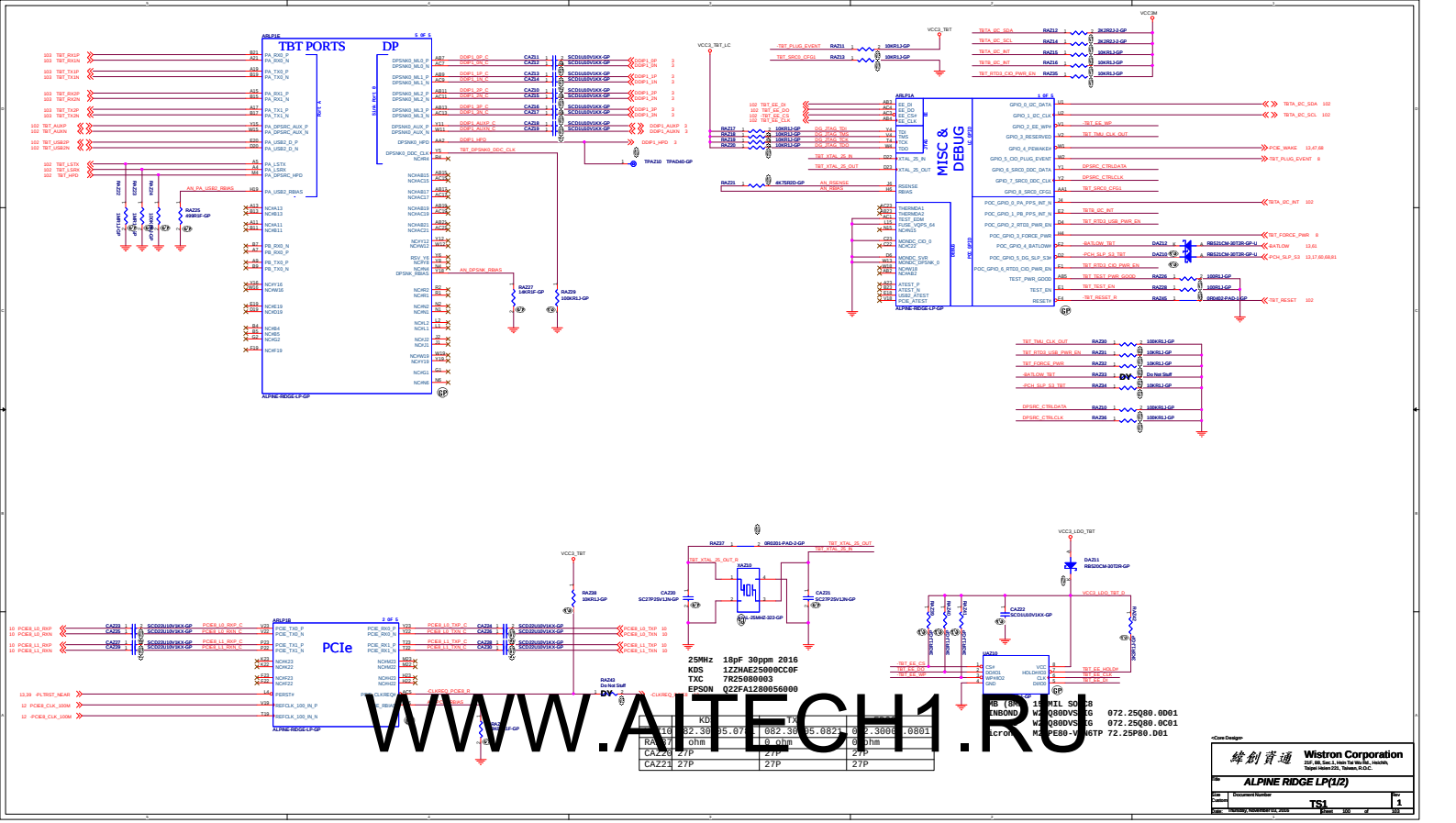

	KD	TX	
RA219	82.3 0ohm	95.0 82.3 0ohm	95.0 82.3 0ohm
CAZ28	27P	27P	27P
CAZ21	27P	27P	27P

MB (8M	11MIL SOP8	
ENBOND	W25Q80DVSSIG	072.25Q80.0D01
	W25Q80DVSSIG	072.25Q80.0C01
Micron	MT25QL80	72.25P80.D01

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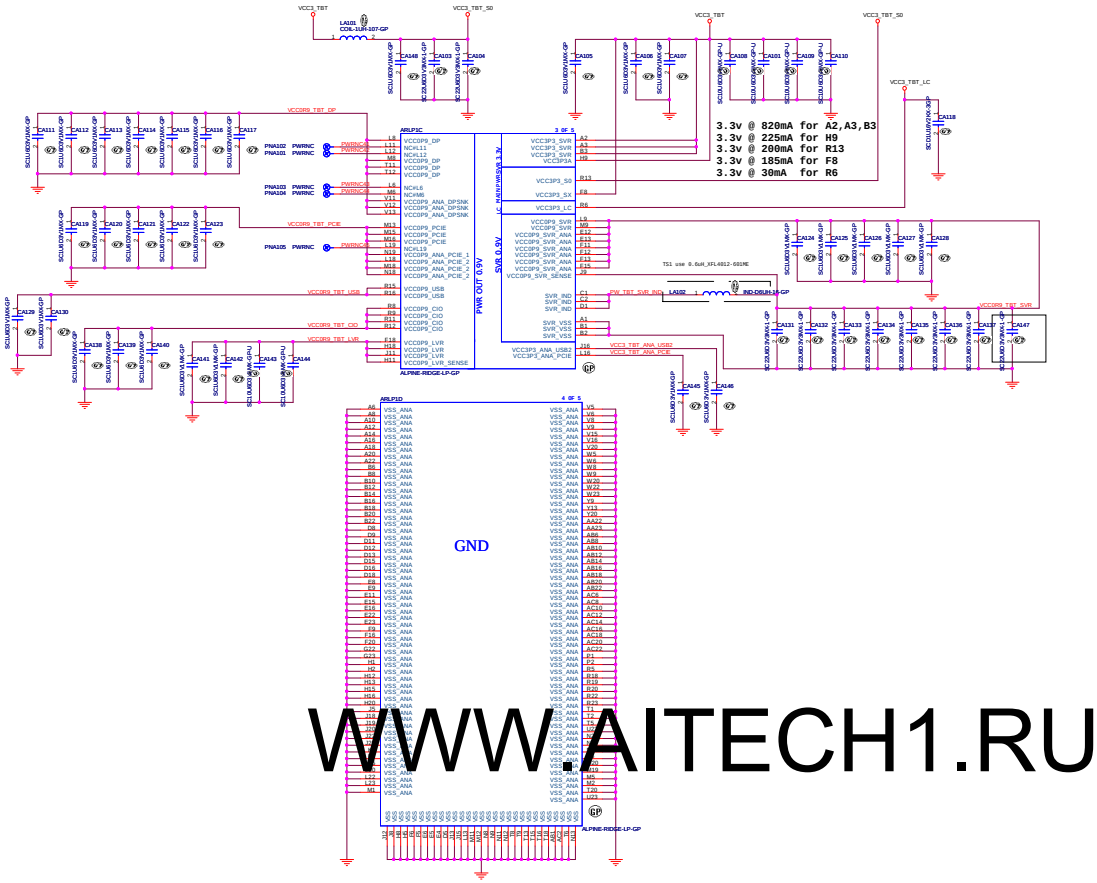
ALPINE RIDGE LP(1/2)

TS1

1



<Core Design>

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: ALPINE RIDGE LP(2/2)		
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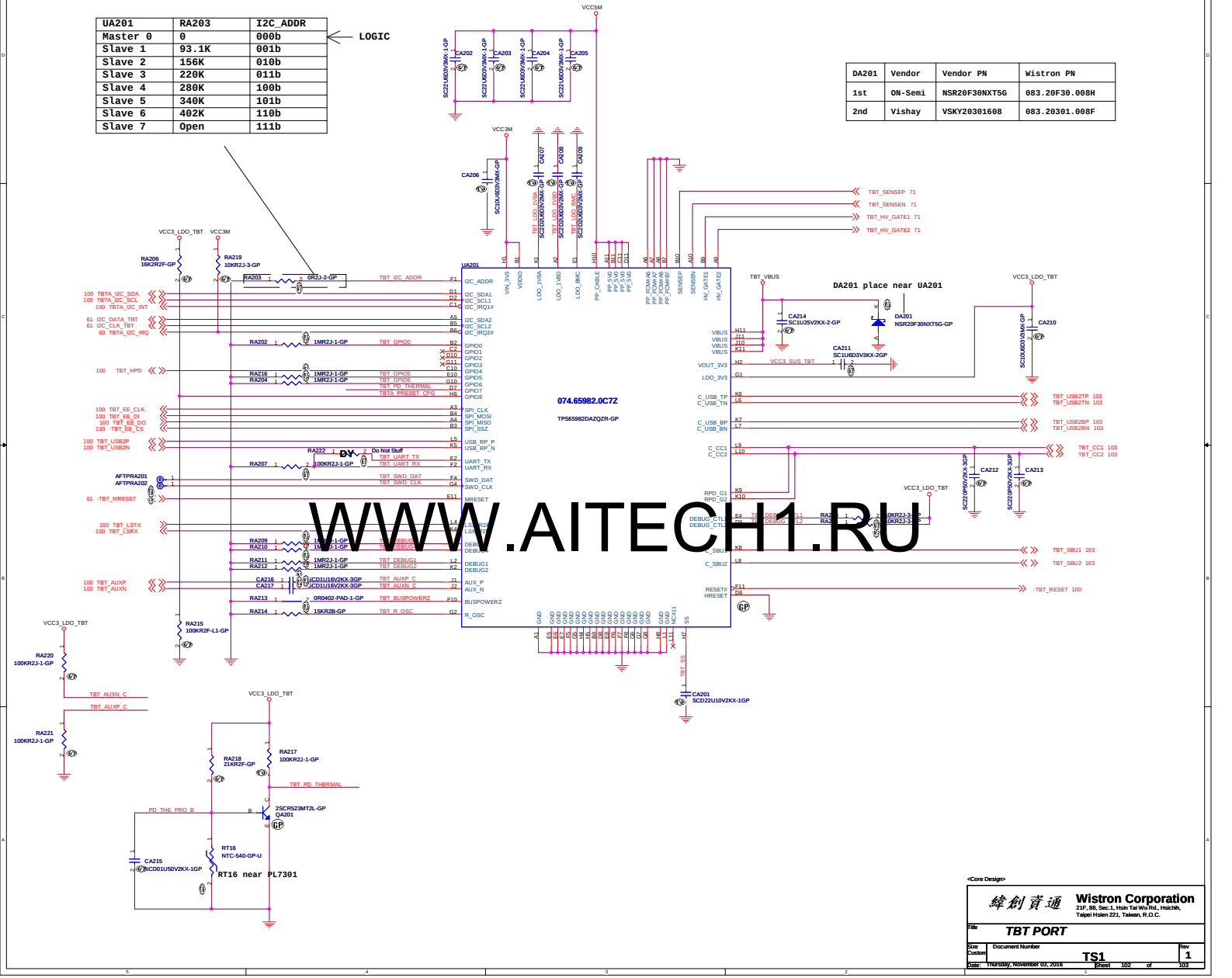
TABLE: TPS65982 I2C Address

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	1	DEBUG_CTL2	DEBUG_CTL1	I2C_ADDR			R/W

UA201	RA203	I2C_ADDR
Master 0	0	000b
Slave 1	93.1K	001b
Slave 2	156K	010b
Slave 3	220K	011b
Slave 4	280K	100b
Slave 5	340K	101b
Slave 6	402K	110b
Slave 7	Open	111b

LOGIC

DA201	Vendor	Vendor PN	Wistron PN
1st	ON-Semi	NSR20F30NXT5G	083.20F30.008H
2nd	Vishay	VSKY20301608	083.20301.008F



<Core Design>

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Title: TBT PORT

Size: Custom | Document Number: TS1 | Rev: 1

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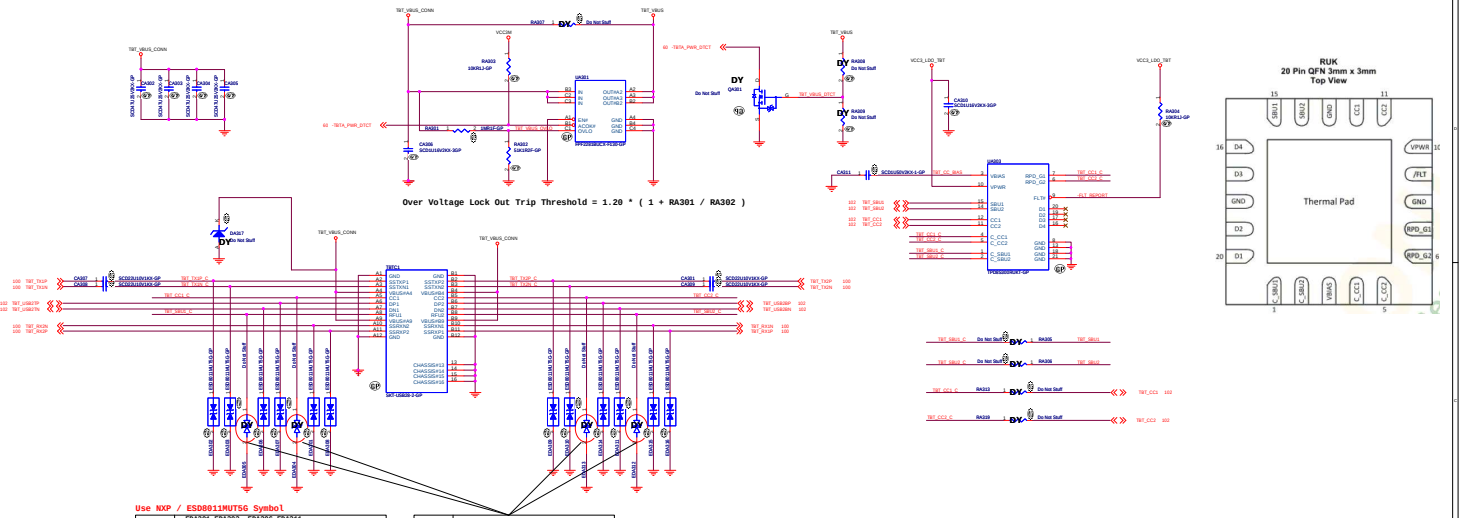

Use NXP / ESD8011MUTSG Symbol

	EDA301-EDA303 ,EDA306-EDA311 EDA314-EDA316
1st	NXP PESD5V0H1BSF 083.5V0H1.00AF
2nd	N/A
3rd	N/A

	EDA304, EDA305, EDA312, EDA313
1st	RClamp2451ZA 083.02451.00A0
2nd	N/A
3rd	N/A

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Title: THUNDERBOLT CONNECTOR

Size: A3 | Document Number: TS1 | Rev: 1

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